Using SoC to Achieve Low Size, Weight, Power and Cost in an Advanced PNT Module

An Altera SoC Application Case Study

Ron Dries, Embedded Software Engineer

Denis Reilly, Lead Engineer

spectracom

Spectracom: GNSS Signal Management

*Spectracom simplifies **Position, Navigation, and Timing** integration into our customer's systems.*

Bringing Technology to:

- *Military, Aerospace*
  - *UAV's*
  - *Electronic Warfare*
  - *C4ISR*
- *High-End Commercial Apps*
  - *Datacenters*
  - *Robotics/Telematics*
  - *IDM*
  - *GIS Data Mining*

ASDF ALTERA SoC DEVELOPERS FORUM

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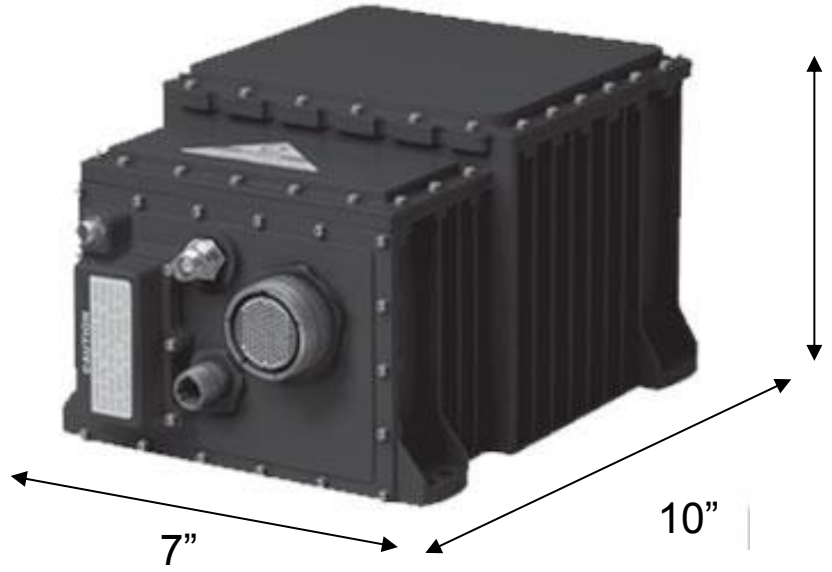
Problem Statement

Shrink functionality of two boxes into one small module for UAVs

- Smallest possible PNT device
- Reduce size by 40x
- Reduce weight by 10x
- Reduce power by 10x
- Maintain the same interfaces



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VersaPNT – Rugged, Airborne PNT Solution – all in one module

- Fully integrated PNT sensor: 3 main components
  - Embedded GNSS receiver
  - Internal Inertial Measurement Unit (IMU)
  - Precision Clock
- GNSS Receiver
  - Civilian or SAASM
  - Multi-constellations – GPS, GLONASS, Galileo, Beidou
- Inertial Navigation System (INS)
  - Internal MEMS device
  - Optional external IMUs
  - 50+ state Extended Kalman Filter (EKF) processing
- Precision Clock
  - Miniature Atomic Clock or OCXO
  - GNSS disciplined

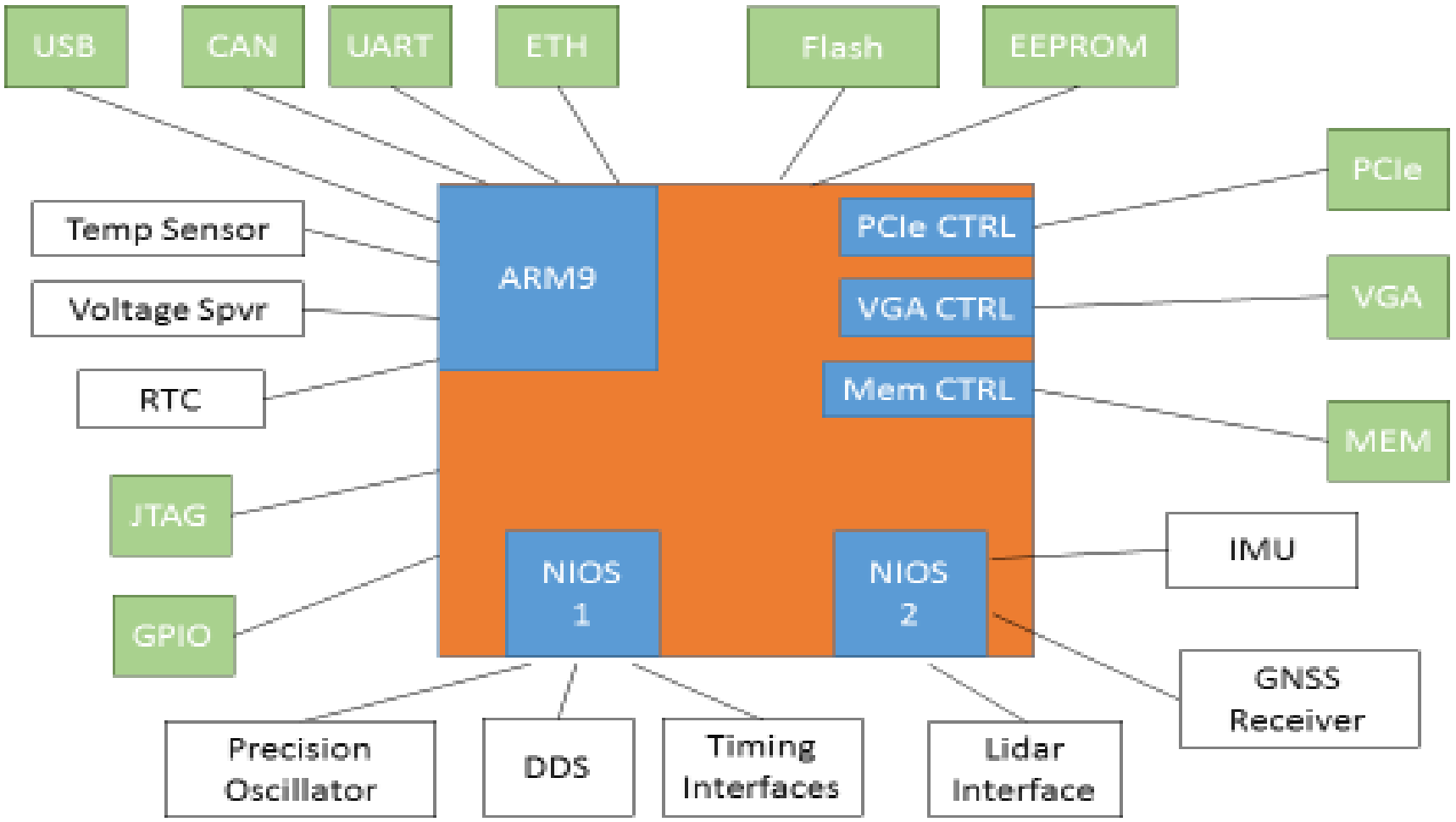
5”

VITA 75 standard rugged enclosure

Why SoC?

- High density, low SWaP (Size, Weight and Power) design
- Multi-processor capability
  - Combining three processors and dedicated FPGA circuitry into a single chip.
- Re-host of established code set and architecture
  - Leveraging proven Navigation and Timing firmware and software
- Wide temperature range, rugged environment
  - MIL-STD-810 requirements
- High reliability
  - Reduced chip count and interconnects increase reliability
  - Targeted for military, security and other mission critical application
- Fast time to market
  - Trial porting of existing codebase during evaluation period proved the feasibility and lowered the project schedule risk

SoC Block Diagram



ARM Cortex A9 Main processor

- controls network and user interfaces
- General supervisory functions

NIOS soft core #1

- Timing function
- Realtime events

NIOS soft core #2

- Positioning and Navigation functions
- Interface to GPS
- Interface to IMU
- Interface to other nav sensors

Highlights of Project

- Multi-processor application
- Specialized timing HW and analog circuitry required
- Realtime processing in FPGA

- Step 1: Prototype feasibility on Altera development board
  - Head start on SW porting
  - Provided development velocity measurement for project planning
- Step 2: Create an evaluation board for development
  - Contains all specialized circuitry
  - Expanded layout for developmental testing
- Step 3: Build final form factor HW
- Step 4: Product qualification testing

FPGA/SoC Hardware Design Highlights

- We replaced the bus interface between systems in our existing product with the Avalon bus.
- We are re-using all of our existing application-specific FPGA code.
- We have tested our DDR interfaces.
- We have demonstrated that we can use the FPGA-to-SDRAM bridge to execute NIOS code in the memory attached to the HPS.
  - It is our job to make sure the NIOS and HPS don't stomp on each others' memory space!
- We have combined a processor module, a second embedded processor, and our FPGA components into one FPGA SoC device.

SW Insights

- Straightforward porting of timing software from Coldfire to NIOS
  - Software architecture allowed for easy transition
  - Software NIOS could be configured to meet software needs.
  - Altera NIOS tools and example programs eased the transition
- Convert Linux driver from PCI to shared memory
  - Previous physically separated processors communicated over PCI
  - SOC allowed the for conversion from PCI to shared memory between NIOS and Cortex A9
- Challenging port of existing Gentoo Linux system
  - Conversion from x86 to ARM needed new development environment
  - Difficulty with configuring Kernel and acquiring drivers for our peripherals
  - Need to maintain support for grub on x86 while also using u-boot on ARM

Evaluation Board

- PCIe bus for peripheral expansion, future product development
- Interfaces and signal test point breakouts
  - Ethernet
  - VGA
  - USB
  - CAN
- Peripherals
  - Precision clock
  - DDS frequency generation
  - Temp sensors

Summary Status and Lessons Learned

- Altera SoC has been a good choice for our rugged airborne design
  - We can meet our low-SWaP requirements
  - We can re-use existing code
- Still a work in process
  - Testing on Evaluation Board now
- Design tools are very good
  - Bus analyzer is built in the FPGA
  - Still need to investigate some purchased debugging tools
  - Good support from Altera and Arrow
- Lots of Linux kernel learning during the port from x86 to ARM
- Altera's SOC Linux vs. our Gentoo distribution
  - Keeping the old distribution is less risky than switching to a new OS
  - Using modified Altera kernel from rocketboards.org

Thank You

ronald.dries@spectracom.orolia.com

denis.reilly@spectracom.orolia.com

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