SPECTRACOM LIMITED WARRANTY

LIMITED WARRANTY

Spectracom warrants each new product manufactured and sold by it to be free from defects in software, material, workmanship, and construction, except for batteries, fuses, or other material normally consumed in operation that may be contained therein AND AS NOTED BELOW, for five years after shipment to the original purchaser (which period is referred to as the “warranty period”). This warranty shall not apply if the product is used contrary to the instructions in its manual or is otherwise subjected to misuse, abnormal operations, accident, lightning or transient surge, repairs or modifications not performed by Spectracom.

The GPS receiver is warranted for one year from date of shipment and subject to the exceptions listed above. The power adaptor, if supplied, is warranted for one year from date of shipment and subject to the exceptions listed above.

THE ANALOG CLOCKS ARE WARRANTED FOR ONE YEAR FROM DATE OF SHIPMENT AND SUBJECT TO THE EXCEPTIONS LISTED ABOVE.

THE TIMECODE READER/GENERATORS ARE WARRANTED FOR ONE YEAR FROM DATE OF SHIPMENT AND SUBJECT TO THE EXCEPTIONS LISTED ABOVE.

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Spectracom’s obligation under this warranty is limited to in-factory service and repair, at Spectracom’s option, of the product or the component thereof, which is found to be defective. If in Spectracom’s judgment the defective condition in a Spectracom product is for a cause listed above for which Spectracom is not responsible, Spectracom will make the repairs or replacement of components and charge its then current price, which buyer agrees to pay.

Spectracom shall not have any warranty obligations if the procedure for warranty claims is not followed. Users must notify Spectracom of the claim with full information as to the claimed defect. Spectracom products shall not be returned unless a return authorization number is issued by Spectracom.

Spectracom products must be returned with the description of the claimed defect and identification of the individual to be contacted if additional information is needed. Spectracom products must be returned properly packed with transportation charges prepaid.

Shipping expense: Expenses incurred for shipping Spectracom products to and from Spectracom (including international customs fees) shall be paid for by the customer, with the following exception. For customers located within the United States, any product repaired by Spectracom under a “warranty repair” will be shipped back to the customer at Spectracom’s expense unless special/faster delivery is requested by customer.

Spectracom highly recommends that prior to returning equipment for service work, our technical support department be contacted to provide trouble shooting assistance while the equipment is still installed. If equipment is returned without first contacting the support department and “no problems are found” during the repair work, an evaluation fee may be charged.

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Extended warranties can be purchased for additional periods beyond the standard five-year warranty. Contact Spectracom no later than the last year of the standard five-year warranty for extended coverage.

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1 Overview

The TPRO-IP is a precision clock that can be read through a host IP carrier. The TPRO-IP automatically synchronizes to standardized time code signals. It is used for time tagging. Time tagging can be done by reading the clock through four 16-bit time registers or by a logic pulse from the outside world (an "external event"). The 16-bit reads are usually used for software initiated time tagging (for example time-tagging the time a block of data transfer starts or completes). Reading the first 16-bit time register (for units of microseconds through units of milliseconds) also freezes the tens of milliseconds through hundreds of days.

External events are usually used for time-tagging hardware related events (for example the exact time of a radar transmit pulse) because the added error of variation in software delays degrades the accuracy or a software initiated time tag. The time tag data for external events is transferred to the host through a byte wide hardware FIFO as a sequence of 10 bytes.

Inputs to the TPRO-IP are modulated timecode, host commands (not usually needed) and external event pulsed as required for the application.

Outputs are DC level shift IRIG-B time code, and a match pulse that occurs at user commanded times. The TPRO-IP also can generate interrupts to the host system as enabled and selected by the host system. Interrupt sources include external event data FIFO not empty and start or stop time match.

The clock will automatically synchronize to specified time code signals. Status bits advise the host of synchronization status. If there is no synchronization source the TPRO-IP will start counting at 000 days ..00 seconds at power-on. The clock time can be set by user commands.

1.1 Inventory

Before installing the board, please verify that all material ordered has been received. If there is a discrepancy, please contact Spectracom Customer Service at US 585.321.5800.

1.2 Inspection and Support

Unpack the equipment and inspect it for damage. If any equipment has been damaged in transit, please contact Spectracom Customer Service at US 585.321.5800.

If any problems occur during installation and configuration of your Spectracom product, please contact Spectracom Technical Support at US 585.321.5823 or US 585.321.5824.

CAUTION: Electronic equipment is sensitive to Electrostatic Discharge (ESD). Observe all ESD precautions and safeguards when handling the timecode generator.
NOTE: If equipment is returned to Spectracom, it must be shipped in its original packing material. Save all packaging material for this purpose.

NOTE: In this manual, the prefix "0x" indicates that the number is in hexadecimal (Base 16) format.
# 2 Specifications

## 2.1 Physical

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>99.06 mm (3.9&quot;) x 45.72 mm (1.8&quot;) (Industry pack size)</td>
</tr>
<tr>
<td>IP bus Type</td>
<td>Single 16-bit</td>
</tr>
<tr>
<td>Power</td>
<td>+5V ± 5%, 100mA typical</td>
</tr>
<tr>
<td></td>
<td>150 mA max.</td>
</tr>
<tr>
<td></td>
<td>+12V ± 5%, 100 mA max</td>
</tr>
<tr>
<td>Temperature</td>
<td>0 to 50 C operation</td>
</tr>
<tr>
<td></td>
<td>-40 to 60 C storage</td>
</tr>
<tr>
<td>Humidity</td>
<td>0 to 95% non-condensing</td>
</tr>
</tbody>
</table>

## 2.2 Timecode Input

<table>
<thead>
<tr>
<th>Code Format</th>
<th>IRIG-B (B122)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplitude (mark)</td>
<td>1.2 Vp-p min, 8.0 Vp-p max</td>
</tr>
<tr>
<td>Polarity</td>
<td>Detected automatically</td>
</tr>
<tr>
<td>Modulation Ratio</td>
<td>2:1 min, 3:1 typ, 4:1 max input</td>
</tr>
<tr>
<td>Impedance</td>
<td>&gt; 10 K ohms</td>
</tr>
<tr>
<td>Input Time Accuracy</td>
<td>Must be better than 100 ppm</td>
</tr>
</tbody>
</table>

## 2.3 Timecode Output

| Code Format                      | DC Level Shift IRIG-B (B002)           |

## 2.4 Time–Tag Input

| Input Voltage                    | -0.5 V min, +0.8 V max for logic 0     |
|                                  | +2.0 V min, +5.5 max for logic 1       |
| Tags rising edge                 |                                        |
| Input Current                    | <5μA for logic 0                       |
|                                 | <5μA for logic 1                       |
| Rise/Fall Time                   | 500 ns max                             |
| Repetition Rate                  | 2000 events per second max timing     |
| Resolution                       | 1 μs                                   |
2.5 On-Board Clock

<table>
<thead>
<tr>
<th>Resolution</th>
<th>1 µs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>366:23:59:59.999999</td>
</tr>
<tr>
<td>Date Format</td>
<td>Integer (001-366)</td>
</tr>
<tr>
<td>Synchronization Time</td>
<td>&lt; 8 seconds</td>
</tr>
</tbody>
</table>

2.6 IP Bus Interface

<table>
<thead>
<tr>
<th>Meets IP specifications per ANSI/VITA-4 1995</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP data Transfer cycles supported</td>
</tr>
<tr>
<td>Input/Output (IOSel*)</td>
</tr>
<tr>
<td>ID Read (IDSEL*)</td>
</tr>
<tr>
<td>Interrupt</td>
</tr>
</tbody>
</table>

2.7 Match Output

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>3.8 V min at 6mA (high)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.4 V max at –6 mA (low)</td>
</tr>
<tr>
<td>Settability</td>
<td>1µs</td>
</tr>
</tbody>
</table>
### 3 Register Assignments and ID Data

#### 3.1 Register Assignments

<table>
<thead>
<tr>
<th>Offset from Base Address</th>
<th>Bits Bit 0 is LSB</th>
<th>Read Usage</th>
<th>Write Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Status</td>
<td>Interrupt Enable</td>
<td>Interrupt Enable</td>
</tr>
<tr>
<td>1</td>
<td>7</td>
<td>FIFO not empty interrupt enable</td>
<td>FIFO not empty interrupt enable</td>
</tr>
<tr>
<td>6</td>
<td>MATCH flag interrupt enable</td>
<td>MATCH flag interrupt enable</td>
<td>MATCH flag interrupt enable</td>
</tr>
<tr>
<td>5</td>
<td>N/U</td>
<td>N/U</td>
<td>N/U</td>
</tr>
<tr>
<td>4</td>
<td>External event enable 1=enable 0=disable set to 0 by reset</td>
<td>External event enable 1=enable 0=disable set to 0 by reset</td>
<td>External event enable 1=enable 0=disable set to 0 by reset</td>
</tr>
<tr>
<td>3</td>
<td>MATCH flag</td>
<td>1 = clear flag 0 = no change</td>
<td>1 = clear flag 0 = no change</td>
</tr>
<tr>
<td>2</td>
<td>In-sync flag 1 = in-sync 0 = non in-sync</td>
<td>Read only</td>
<td>Read only</td>
</tr>
<tr>
<td>1</td>
<td>Time code input decodable flag 1 = decodable 0 = not decodable</td>
<td>Read only</td>
<td>Read only</td>
</tr>
<tr>
<td>0</td>
<td>FIFO empty flag 0 = empty 1 = not empty</td>
<td>Read only</td>
<td>Read only</td>
</tr>
<tr>
<td>3</td>
<td>7..0 Data FIFO Command Port</td>
<td>Command Port</td>
<td>Command Port</td>
</tr>
<tr>
<td>5</td>
<td>7..0 Interrupt vector</td>
<td>Interrupt vector</td>
<td>Interrupt vector</td>
</tr>
<tr>
<td>9</td>
<td>7..0 N/U Simulate external event (write any data pattern)</td>
<td>Simulate external event (write any data pattern)</td>
<td>Simulate external event (write any data pattern)</td>
</tr>
<tr>
<td>D</td>
<td>7..0 N/U Reset FIFO and release microcomputer reset</td>
<td>Reset FIFO and release microcomputer reset</td>
<td>Reset FIFO and release microcomputer reset</td>
</tr>
<tr>
<td>F</td>
<td>7..0 N/U Assert microcomputer reset</td>
<td>Assert microcomputer reset</td>
<td>Assert microcomputer reset</td>
</tr>
<tr>
<td>8</td>
<td>15..0 (WORD) Time (10^3 µS..10^0 µS) Reading this word latches higher order words</td>
<td>N/U</td>
<td>N/U</td>
</tr>
<tr>
<td>A</td>
<td>15..0 (WORD) Time (seconds &amp; 100s, 10s or milliseconds)</td>
<td>N/U</td>
<td>N/U</td>
</tr>
<tr>
<td>C</td>
<td>15..0 (WORD) Time (hours &amp; minutes)</td>
<td>N/U</td>
<td>N/U</td>
</tr>
<tr>
<td>E</td>
<td>15..0 (WORD) Time (days)</td>
<td>N/U</td>
<td>N/U</td>
</tr>
</tbody>
</table>
### 3.2 ID Data

<table>
<thead>
<tr>
<th>Offset from Base Address</th>
<th>Contents</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>81</td>
<td>49</td>
<td>ASCII &quot;I&quot;</td>
</tr>
<tr>
<td>83</td>
<td>50</td>
<td>ASCII &quot;P&quot;</td>
</tr>
<tr>
<td>85</td>
<td>41</td>
<td>ASCII &quot;A&quot;</td>
</tr>
<tr>
<td>87</td>
<td>43</td>
<td>ASCII &quot;C&quot;</td>
</tr>
<tr>
<td>89</td>
<td>4F</td>
<td>ID</td>
</tr>
<tr>
<td>8B</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>8D</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>8F</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>93</td>
<td>0C</td>
<td>ID SIZE</td>
</tr>
<tr>
<td>95</td>
<td>CE</td>
<td>CRC</td>
</tr>
</tbody>
</table>
4 Configuration

4.1 Input/output connections
For modulated IRIG-B input operation:

Connect the modulated IRIG-A or IRIG-B source to the IP carrier header pin 1 and the signal ground to pin 2.

Connect the diagnostic LED anode (long lead) to pin 22 and the cathode (short lead) to pin 23.

If using external event input, connect it to pin 9. Else ground pin 9 to pin 10.

Connect pin 31 to pin 32 so IPPS TTL level input doesn't float.

4.2 Base address
The base address of the TPRO-IP in user host space is determined by configuration of the IP carrier and by which slot in the IP carrier the TPRO-IP is placed. For example, the Greenspring Computers VIPC310 VME bus dual IP carrier has a factory default base address of 6000 (for IP slot A) in A16 space.

4.3 Interrupt Request Level
The host bus interrupt level associated with the IRQ0 level signal generated by the TPRO-IP is determined by configuration of the IP carrier. For example, the Greenspring Computers VIPC310 VME bus dual IP carrier has a factory default VME bus IRQ41 for slot A and IRQ2L for slot B.
5 Installation

NOTE: Before installing the TPRO-IP in your system, please make a record of the serial number, the PWB Revision level (example A1 or A), the firmware version labeled on EPROM U3 (example: 4A274A22), and the version labels on FPGA device U5 (example: 4B01A). This information is required for telephone support of the product. Please make the record known to anyone who may require support.

CAUTION: Observe all ESD procedures when handling the board and the computer. Before installing the board, discharge static buildup by touching the metal frame of the computer with one hand and the protective bag containing the board with the other hand. Open the protective bag only after static buildup has been safely discharged.

Shut down the system.

Install the TPRO-IP board in a IP carrier slot. The TPRO-IP has inputs and outputs that should be connected for the users requirements. There are up to two inputs from the external world: input time code (if used) and a TTL external event pulse (if used). For the TPRO-IP, if input time code is not provided, the board will provide "local" timing starting at 000 days, 00 hours, 00 minutes, 00 seconds. The external event pulses may come from external user equipment, or pulse outputs from the TPRO-IP may be looped back and used as external event inputs with a simple jumper connection. Custom factory configurations will have a manual addendum detailing non-standard I/O configuration.

Start the system.
6 Board Operation

6.1 General

The TPRO-IP operates automatically as soon as the host computer system does the power-on reset. To change the operating parameters or read data consult the Programming section. A status LED can be connected to the 50-pin IP carrier I/O connector for flashing a status pattern to assist in diagnosing installation errors. The pattern is a sequence of short and long flasher. Trailing short flashes are deleted so the status pattern can repeat more frequently.

<table>
<thead>
<tr>
<th>Flash Position</th>
<th>Meaning of short (cleared) flash</th>
<th>Meaning of long (set) flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modulated timecode input being used for time reference</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Synchronization to better than 5 μS verified with last 5 seconds</td>
<td>Synchronization to better than 5 μS not verified within last 5 seconds</td>
</tr>
<tr>
<td>3</td>
<td>In applications with modulated time code inputs only, this status bit will always be set</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>In applications with modulated timecode inputs only, this status bit will always be set</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>In applications with modulated time code inputs only, this status bit will always be set</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Timecode input being decoded</td>
<td>Timecode input not decodable. In applications without modulated timecode inputs, this status bit will always be set</td>
</tr>
</tbody>
</table>

6.2 Propagation Delay Adjustment

Depending on the actual absolute time accuracy required in the user’s application, the TPRO-IP may be commanded to correct for the time required for the time code signal to travel the distance between the time code source and the IP host computer. This delay time is called "propagation delay time" and is about 3.3 microseconds per kilometer for radio time code transmission and about 5 μS per kilometer for copper wire transmission. There is also a time delay on the order of 25 μS that may be caused by small phase shifts due to reactance’s at the time code input. To correct for propagation delay, the TPRO-IP can use a propagation delay correction setting ranging between -1000 (because sometime sources transmit early) and +8999 μS. The default setting is 0 μS after the TPRO-IP is reset at power-on or after a RESET command from the user. Users can change the setting by a sequence of programmed commands to the command register on the TPRO-IP. If absolute microsecond accuracy is required, the user will probably need to calibrate the TPRO-IP when it is installed for propagation delay correction by comparing the on-board clock time with a portable reference. The correct propagation delay correction setting is converted on rapidly by trial and error. This setting will not need to be changed unless the location or cabling of the installation is changed. Determining the correct propagation delay setting will probably need the help or a special user program to let various propagation delay settings be tried experimentally while zeroing in on the correct setting. The normal user program should have the capability of using the correct setting once it is determined.
# 7 Pinouts

## 7.1 50 Pin IP Carrier Header (P1) Input/Output Pinout

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ground</td>
</tr>
<tr>
<td>2</td>
<td>System Clock 8 MHz</td>
</tr>
<tr>
<td>3</td>
<td>Reset Low</td>
</tr>
<tr>
<td>4-19</td>
<td>SD0-SD15</td>
</tr>
<tr>
<td>20</td>
<td>BS0 Low</td>
</tr>
<tr>
<td>21</td>
<td>BS1 Low</td>
</tr>
<tr>
<td>22</td>
<td>-12V</td>
</tr>
<tr>
<td>23</td>
<td>+12V</td>
</tr>
<tr>
<td>24</td>
<td>+5V</td>
</tr>
<tr>
<td>25-26</td>
<td>Ground</td>
</tr>
<tr>
<td>27</td>
<td>+5V</td>
</tr>
<tr>
<td>28</td>
<td>System Read Write Low</td>
</tr>
<tr>
<td>29</td>
<td>ID Select</td>
</tr>
<tr>
<td>30</td>
<td>Not Used</td>
</tr>
<tr>
<td>31</td>
<td>Memory Select</td>
</tr>
<tr>
<td>32</td>
<td>Not Used</td>
</tr>
<tr>
<td>33</td>
<td>Interrupt Select</td>
</tr>
<tr>
<td>34</td>
<td>Not Used</td>
</tr>
<tr>
<td>35</td>
<td>Input/Output Select</td>
</tr>
<tr>
<td>36</td>
<td>Reserved</td>
</tr>
<tr>
<td>37</td>
<td>SA1</td>
</tr>
<tr>
<td>38</td>
<td>Not Used</td>
</tr>
<tr>
<td>39</td>
<td>SA2</td>
</tr>
<tr>
<td>40</td>
<td>Not Used</td>
</tr>
<tr>
<td>41</td>
<td>SA3</td>
</tr>
<tr>
<td>42</td>
<td>Interrupt Request 0 Low</td>
</tr>
<tr>
<td>43</td>
<td>SA4</td>
</tr>
<tr>
<td>44</td>
<td>Interrupt Request 1 Low</td>
</tr>
<tr>
<td>45</td>
<td>SA5</td>
</tr>
<tr>
<td>46</td>
<td>Not Used</td>
</tr>
<tr>
<td>47</td>
<td>SA6</td>
</tr>
<tr>
<td>48</td>
<td>ACK Low</td>
</tr>
<tr>
<td>49</td>
<td>Reserved</td>
</tr>
<tr>
<td>50</td>
<td>Ground</td>
</tr>
</tbody>
</table>
### 7.2 50 Pin IP Carrier Header (P2)

<table>
<thead>
<tr>
<th>PIN</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modulated timecode input</td>
</tr>
<tr>
<td>2</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>4,6</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>5,7</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>8</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>9</td>
<td>External event (positive going edge) TTL level input</td>
</tr>
<tr>
<td>10</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>12</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>13</td>
<td>Spare output #1 for future customization</td>
</tr>
<tr>
<td>14</td>
<td>Ground</td>
</tr>
<tr>
<td>15</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>16</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>17</td>
<td>Spare output #2 for future customization</td>
</tr>
<tr>
<td>18</td>
<td>Ground</td>
</tr>
<tr>
<td>19</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>20</td>
<td>Ground</td>
</tr>
<tr>
<td>21</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>22</td>
<td>+5V output for anode side of diagnostic LED. LED must have internal current limiting resistor. <strong>WARNING:</strong> Users should exert extreme care in connections to pin 22. Shorting pin 22 to ground or +12V can damage the TPRO-IP or the host system.</td>
</tr>
<tr>
<td>23</td>
<td>Cathode side of diagnostic LED</td>
</tr>
<tr>
<td>24</td>
<td>Ground</td>
</tr>
<tr>
<td>25</td>
<td>+12V output <strong>WARNING:</strong> Users should exert extreme care in connections to pin 25. Shorting pin 25 to ground or +5V can damage the TPRO-IP or the host system.</td>
</tr>
<tr>
<td>26</td>
<td>SPARE3 input for future customization</td>
</tr>
<tr>
<td>27</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>28,30</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>29</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>31</td>
<td>Ground side of 47 ohm termination resistor connected to pin 4, 6. Connect to pin 32 to terminate pin 4 or 6 in 47 ohm resistor</td>
</tr>
<tr>
<td>32</td>
<td>Ground</td>
</tr>
<tr>
<td>33</td>
<td>IRIG-A future customization option. Connects to pin 34 for IRIG-A input</td>
</tr>
<tr>
<td>34</td>
<td>IRIG-A future customization option. Connects to pin 33 for IRIG-A input</td>
</tr>
<tr>
<td>35,37</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>36</td>
<td>Not used. User should not make connection to these pins.</td>
</tr>
<tr>
<td>38</td>
<td>IRIG-B DC level shift TTL output</td>
</tr>
<tr>
<td>39</td>
<td>MATCH signal TTL level output</td>
</tr>
<tr>
<td>40</td>
<td>GATES signal TTL level output</td>
</tr>
<tr>
<td>41-50</td>
<td>Microprocessor signal connections for logical analyzer User should make no connections to pins 41-50</td>
</tr>
</tbody>
</table>
8 Programming

User programs interface to hardware and firmware functions of the TPRO-IP. The hardware functions used are:

- Reading the clock through the 16 bit registers
- Reading the status register
- Initializing the data FIFO
- Reading the data FIFO to read external event time tags or command responses
- Enabling/disabling interrupts
- Forcing hardware reset

Firmware functions are initiated by writing 8 bit commands to the command port of the TPRO-IP.

Test programs in the Appendix (Page 36) show examples of these functions.

8.1 Reading the clock through the 16-bit registers

To measure the instantaneous time, a program first does a work I/O read from the low order 16 bit time register at base address + 8. When the low order register is read, the 3 high order time words are stored at the same time in an internal registers in the TPRO-IP. The 3 registers will be frozen until the low order time register is read again. So, whenever the high order registers are read, the time that is returned is the time when the low order register was last read. Any (or none) of the 3 high order registers may be read according to the user's application.

<table>
<thead>
<tr>
<th>Bits</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>$10^3 \mu S$ BCD</td>
<td>$10^2 \mu S$ BCD</td>
<td>$10^1 \mu S$ BCD</td>
<td>$10^0 \mu S$ BCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Data organization (base address + offset 8)

<table>
<thead>
<tr>
<th>Bits</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>10 second BCD</td>
<td>1 second BCD</td>
<td>$10^3 \mu S$ BCD</td>
<td>$10^4 \mu S$ BCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Data organization (base address + offset A)

<table>
<thead>
<tr>
<th>Bits</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>10 hour BCD</td>
<td>1 hour BCD</td>
<td>10 minute BCD</td>
<td>1 minute BCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

16-bit word data organization (base address + offset C)

<table>
<thead>
<tr>
<th>Bits</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>0</td>
<td>$10^2$ days BCD</td>
<td>10 day BCD</td>
<td>1 day BCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Data organization (base address + offset E)
8.2 Status

The meaning of the status bits is defined in the Specifications section of this manual. The Match Interrupt Enable, FIFO Not Empty Interrupt, External Event Enable and Match Flag bits are Read/Write, while all others are read only.

8.3 FIFO Initialization

When a user program starts using the TPRO-IP there may be stale external event or command response data in the FIFO. To initialize the FIFO the user can do a write (any data) to the FIFO Reset port, or the user can just read the FIFO 512 times. Right after initialization, the user should check the FIFO Empty Flag for "0" in case an external event just happened while initializing. Once initialization is done, it does NOT need to be done again so long as the user program makes sure that any data put in the FIFO (in response to external events or user commands) is emptied out by user programs.

8.4 Reading the FIFO

The user program should ALWAYS check the FIFO EMPTY flag (bit 0) for "1" before reading a byte from the FIFO. Otherwise user programs may be reading FIFO data out faster than the TPRO-IP firmware is writing data into the FIFO. Data is always written in 10 byte groups to the FIFO by the TPRO-IP firmware.

8.5 External Event Time Tagging

The External Event Enable bit (Bit 4 in the Status Register) must be a "1" for External Event Time Tags to occur. The enable bit will be cleared by a power on or programmed RESET. Once set to "1" the Enable bit will stay at "1" until written to "0" or a reset occurs.

In response to a rising edge at the external event input (pin 9 on the 50-pin IP header), the TPRO-IP copies the 10 bytes of time data into the on-board FIFO. It takes about 50 µseconds until the last of the 10 bytes is copied into the FIFO. The transfer time fluctuates because the microcomputer may be interrupted while putting data in the FIFO. The time data is accurate to the exact µsecond when the event occurred and the accuracy is not affected by the transfer time.

The occurrence of an external event pulse can be simulated by doing a byte I/O write (any data value) to base address + 3. The simulated external event does not require that the External Event Enable bit in the Status Register be set.
The host program reads captured time information (100s of days through units of microseconds - a total of 10 bytes) sequentially from the FIFO through the TPRO-IP bus interface. Handshaking is done by the host testing the FIFO NOT EMPTY bit (bit 0) of the TPRO-IP status register (base + 1) for "1" before each byte is read from the data FIFO (base + 3). The data format for FIFO time stamps is:

<table>
<thead>
<tr>
<th>Byte</th>
<th>High Nibble</th>
<th>Low Nibble</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>not defined</td>
<td>not defined</td>
</tr>
<tr>
<td>1</td>
<td>not defined</td>
<td>defined</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>10^2 days</td>
</tr>
<tr>
<td>3</td>
<td>10^1 days</td>
<td>10^6 days</td>
</tr>
<tr>
<td>4</td>
<td>10^1 hours</td>
<td>10^9 hours</td>
</tr>
<tr>
<td>5</td>
<td>10^1 minutes</td>
<td>10^5 minutes</td>
</tr>
<tr>
<td>6</td>
<td>10^1 seconds</td>
<td>10^5 seconds</td>
</tr>
<tr>
<td>7</td>
<td>10^5 µseconds</td>
<td>10^4 µseconds</td>
</tr>
<tr>
<td>8</td>
<td>10^3 µseconds</td>
<td>10^2 µseconds</td>
</tr>
<tr>
<td>9</td>
<td>10^1 µseconds</td>
<td>10^0 µseconds</td>
</tr>
</tbody>
</table>

### 8.6 Interrupts

The host bus interrupt vector is set by writing to the TPRO-IP base address + 5. The TPRO-IP may be programmed to request interrupts at IRQ0 level upon selectable conditions. Interrupts may be enabled by writing a "1" into the corresponding interrupt enable bit in base address + 1.

<table>
<thead>
<tr>
<th>Interrupt Condition</th>
<th>Condition Asserted By</th>
<th>User Action to Deassert Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO not empty</td>
<td>External event or user command causes on board microprocessor to write data into FIFO</td>
<td>I/O read data from FIFO until FIFO empty or write to FIFO reset port</td>
</tr>
<tr>
<td>Match Flag Set</td>
<td>User programmed START or STOP MATCH time is detected</td>
<td>I/O write to base +1 with bit 3 = 1</td>
</tr>
</tbody>
</table>

### 8.7 Forcing Hardware Reset

The user can reproduce the effect of the host power on reset on the TPRO-IP by writing (any data) to the Assert Microprocessor Reset port (base + F). The RESET will remain asserted until the user writes (any data) to the Reset FIFO port (base + D).
8.8 Commands

Commands are sent as a sequence of bytes to the TPRO-IP command register (base address + 3). All commands should be spaced at least 100 µsec apart so the TPRO-IP firmware has enough time to handle each command. An easy way to generate a processor speed independent 100µsec time delay is to read the TPRO-IP status register 100 times. Without any commands, on cold or warm start the TPRO-IP will automatically synchronize to a modulated time code input. There are commands for:

- Setting time
- Setting propagation delay correction for modulated code input
- Disabling synchronization to input
- Re-enabling synchronization to input
- Simulating power-on reset of TPRO-IP firmware
- Setting MATCH START and MATCH STOP times

<table>
<thead>
<tr>
<th>Command</th>
<th>Hi Nibble</th>
<th>Lo Nibble</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set time set register 10³ µS</td>
<td>0</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10² µS</td>
<td>1</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10¹ µS</td>
<td>2</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10⁰ µS</td>
<td>3</td>
<td>0-9</td>
</tr>
<tr>
<td>Set next 1pps time</td>
<td>4</td>
<td>C</td>
</tr>
<tr>
<td>Enable resync</td>
<td>4</td>
<td>D</td>
</tr>
<tr>
<td>Disable sync</td>
<td>4</td>
<td>E</td>
</tr>
<tr>
<td>Reset TPRO-IP firmware</td>
<td>4</td>
<td>F</td>
</tr>
<tr>
<td>Set time set register 102 days</td>
<td>5</td>
<td>0-3</td>
</tr>
<tr>
<td>Report cog/sog/sats</td>
<td>5</td>
<td>C</td>
</tr>
<tr>
<td>Report altitude</td>
<td>5</td>
<td>D</td>
</tr>
<tr>
<td>Report longitude</td>
<td>5</td>
<td>E</td>
</tr>
<tr>
<td>Report latitude</td>
<td>5</td>
<td>F</td>
</tr>
<tr>
<td>Set time set register 10¹ days</td>
<td>6</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10⁰ DAYS</td>
<td>7</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10⁰ HOURS</td>
<td>8</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10⁰ HOURS</td>
<td>9</td>
<td>0-9</td>
</tr>
<tr>
<td>Set time set register 10⁰ MINUTES</td>
<td>A</td>
<td>0-F</td>
</tr>
<tr>
<td>Set time set register 10⁰ MINUTES</td>
<td>B</td>
<td>0-F</td>
</tr>
<tr>
<td>Set time set register 10¹ SECONDS</td>
<td>C</td>
<td>0-F</td>
</tr>
<tr>
<td>Set time set register 10⁰ SECONDS</td>
<td>D</td>
<td>0-F</td>
</tr>
<tr>
<td>Copy time set register to clock time</td>
<td>E</td>
<td>0</td>
</tr>
<tr>
<td>Copy time set register to start/stop hold</td>
<td>E</td>
<td>1</td>
</tr>
<tr>
<td>Copy start/stop hold to start match register</td>
<td>E</td>
<td>2</td>
</tr>
<tr>
<td>and time set register (days.seconds) to start µS</td>
<td>E</td>
<td>3</td>
</tr>
<tr>
<td>Copy start/stop hold to stop match register</td>
<td>E</td>
<td>4</td>
</tr>
<tr>
<td>and time set register (hours,minutes,seconds) to stop µS</td>
<td>E</td>
<td>9</td>
</tr>
<tr>
<td>Clear match flag</td>
<td>E</td>
<td>4</td>
</tr>
<tr>
<td>Report firmware ID in FIFO</td>
<td>E</td>
<td>9</td>
</tr>
<tr>
<td>Clear set time register</td>
<td>F</td>
<td>0</td>
</tr>
</tbody>
</table>
8.9 Setting Time

The user may set the TPRO-IP for applications where the input reference is not used to be used. If the user does not preset a time, a default preset of 0 days through seconds is used. Setting time will usually be preceded by disabling input synchronization. Otherwise, the TPRO-IP firmware will just switch back from the commanded time to the input time as soon as the input is validated. The sequence of commands for setting time is:

Send CLEAR TIME SET REGISTER command (F0h)
Send SET TIME SET REGISTER commands (5<bcd> through 8<BCD>) for 102 days through 10^8 seconds in any order
Send COPY TIME SET REGISTER command (E0h)

At least 100 µS should be allowed between sending each command byte. For example to set time to 123 days 01 hours 23 minutes 45 seconds, the sequence F0 51 62 73 80 91 A2 B3 C4 D5 E0 would be sent. As each SET TIME SET REGISTER command is sent, the corresponding digit in an internal time set buffer in the TPRO-IP will be set. When the COPY TIME SET REGISTER command (E0) is received; the time set buffer will be copied to the clock.

8.10 Setting Propagation Delay Correction

The user may set the compensation for propagation delay between the time code source and the TPRO-IP location. On cold or warm start, the TPRO-IP will assume a propagation delay correction of 0 µS. The sequence of commands for setting propagation delay correction is:

1. Send CLEAR TIME SET REGISTER command (F0h)
2. Send SET TIME SET REGISTER commands (0<bcd> to 3<bcd>)
   For 10^3 µS, 10^2 µS, 10^1 µS, 10^0µS, digits in any order
3. Send SET COPY TIME SET REGISTER command (E0h)

Remember to delay at least 100 µS between sending each command byte. For example to set a propagation delay correction value of 1234 µS, the sequence F0 31 22 13 04 E0 would be sent. Some central timing facilities transmit time codes advanced by 1 millisecond. To correct for the advanced time code, it may be desirable to use a negative propagation delay correction setting. Propagation delay settings of 9000 µS to 9999 µS are used to set NEGATIVE propagation delay correction values of -1000 µS to -1µS respectively. For example, to set -500 µS use a setting of 9500 µS. So, the propagation delay correction range of the TPRO-IP is –1000 µS to +8999 µS.

The TPRO-IP can distinguish between COPY TIME SET commands used for setting propagation delay and COPY TIME SET commands used for setting time by noting that different intervening commands have occurred after the CLEAR TIME SET REGISTER command.

8.11 Disabling Synchronization to Input

To prevent the TPRO-IP from synchronizing its time to input signals, send the DISABLE RESYNC (4Eh) command to the TPRO-IP. This is normally used when you set the TPRO-IP time using the Set Generation Time procedure.
8.12 Re-enabling Synchronization to Input
To release the TPRO-IP from a DISABLE RESYNC command, send the ENABLE RESYNC (4Dh) command to the TPRO-IP. The cold or warm start condition for the TPRO-IP is resync enabled.

8.13 Simulating Power-on Reset of TPRO-IP Firmware
The RESET (4Fh) command to the TPRO-IP rests the on-board Z80 microcomputer.
9 Preventive Maintenance & Troubleshooting

9.1 Oscillator Aging Adjustment

**NOTE:** Applies only to models equipped with -O option ovenized oscillator.

The Oscillator aging adjustment for the TPRO-IP corrects for the effects of aging on the natural crystal oscillator frequency to insure that the undisciplined frequency of the 10 MHz oscillator is 10.000000 MHz ± 10 Hz.

This preventive maintenance should be once every 2 years.

You will need

- A digital frequency counter with 1 PPM or better accuracy and 1 HZ or better resolution (be sure that the counter is calibrated)
- A small screwdriver

If you have a custom crystal oscillator in your unit, consult the oscillator data sheet for adjustment method.

Extend the carrier module on which the TPRO-IP is mounted.

Connect a calibrated frequency counter to the 10 MHz signal at XO1 pin 8.

Power the system up and wait at least five minutes for the on-board crystal oven temperature to stabilize. Then adjust R10 (using the "solder side" access hole) for 10MHz±10Hz. If R10 is not present, you do not have the -O option and cannot adjust the oscillator.

Power down your system, and reinstall carrier without extender.

9.2 Troubleshooting

9.2.1 Before you contact Spectracom

Have the serial number, Rev level, firmware and FPGA ID you were instructed to record during installation. Please include them in any faxes. Try to exhibit the problem in as reduced (fewest boards in the system) configuration as you can. Try to run our examples, modified as little as possible, to be sure that what you think is a hardware problem is really a software problem.

9.2.2 Bus Crashes

If your program crashes due to a bus error when trying to access the TPRO-IP your problem may be:

Board address configured for IP carrier slot used by TPRO-IP doesn’t agree with what your program uses.
9.2.3 Bad data from 16bit data registers

If your program doesn't crash but gets crazy (illegal BCD etc) data from the 16 bit registers your problem may be:

- You are using an address that maps into a different host bus device. To check this hypothesis, remove the TPRO-IP from the IP carrier. If you still can access data from the same address, you are not addressing the TPRO-IP.
- You are using a base address that maps into both the TPRO-IP and another host bus device.
- You are accessing high order bits at base +A, +C, or +E before freezing & reading low order bits at base +8.
- You are reading data (especially if there's lots or zeros) before the TPRO-IP has synchronized to the input code. Remember that there is about a 20-second delay from power on before the TPRO-IP jam syncs to the input code.
- You did a TIME SET command sequence with crazy values.

9.2.4 Bad data from FIFO port

If your program doesn't crash, but has crazy (illegal BCD etc) data from the FIFO your problem may be:

- Your code doesn't check the FIFO NOT EMPTY bit in the STATUS REGISTER for "1" before reading each byte from the FIFO. If your data contains "00" or seems to slip (hours show up where you expected minute's etc) this is very likely the reason.
- You are reading data (especially if there's lots of zeros) before the TPRO-IP has synchronized to the input code. Remember that here is about a 20-second delay from power on before the TPRO-IP jam syncs to the input code. You did a TIME SET command sequence with crazy values.
- You are using an address that maps into memory or into a different device.

9.2.5 Interrupt crashes

Make sure that the interrupt vector register is correctly initialized.

Make sure that the host bus IRQ level agrees with the configuration of the IP carrier for the slot in which the TPRO-IP is installed.

If you are using the FIFO NOT EMPTY interrupt selection, disable the interrupt enable either at the TPRO-IP or at the host interrupt controller while reading the FIFO or you may caused nested FIFO NOT EMPTY interrupts as each byte is read from the FIFO and the IRQ line toggles.
9.2.6 Board never syncs to input code

If the "in-sync" status bit is "0" (indicating an error):

In-sync should be "0" in many cases. A "0" does not mean that there is a fault in the board. Remember that there is about a 20 second delay from power on before the TPRO-IP jam syncs to the input code.

Does the diagnostic LED indicate decodable input signal? If not, the TPRO-IP doesn’t see a signal that it can decode. Check signal amplitude and connections.

Examine the input signal on an oscilloscope and make sure that it meets the input specifications of the TPRO-IP.

Is the time code carrier frequency stable to ±100 PPM? Does it make periodic large (larger than 5 µS) time jumps? Tape playback is very likely to have high frequency error unless you use a calibrated servo track to accurately control speed.
9.3 **Firmware Sample Code**

```
00FF 0000  ILLEGAL   EQU  $FF0000
00FF 6001  IPSTS    EQU  $FF6001
0000 0000  BSTSOR   EQU  0 BIT0: FIFO NOT EMPTY  READ ONLY.
0000 0001  BSIGOK   EQU  1 BIT1: INPUT TIME CODE DECODEABLE. READ ONLY
0000 0002  BSYNCOK  EQU  2 BIT2: GOOD SYNC  READ ONLY
0000 0003  BMAT     EQU  3 BIT3: MATCH STATUS. READ ONLY
0000 0004  BEXTENB  EQU  4 BIT6: EXTERNAL EVENT ENABLE. READ/WRITE
0000 0006  BMATIE   EQU  6 BIT4: MATCH INTERRUPT ENABLE. READ/WRITE
0000 0007  BORIE    EQU  7 BIT7: FIFO NOT EMPTY INTR ENABLE. READ/WRITE
00FF 6003  IPCMD    EQU  $FF6003 COMMAND PORT (WRITE ONLY)
00FF 6003  IPFIFO   EQU  $FF6003 FIFO DATA PORT (READ ONLY)
00FF 6005  IPVEC    EQU  $FF6005 INTR VECTOR FOR IRQ0 (READ/WRITE)
00FF 6009  IPFIFR   EQU  $FF6009 FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
00FF 600D  IPFIO    EQU  $FF600D A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
00FF 600E  IPRESET  EQU  $FF600E A16 BUS WINDOW FOR MVME133+BASE+E OFFSET
00FF 6081  IPID     EQU  $FF6081 ID DATA. SEE IDCHK FOR CORRECT CONTENTS

000000  27C 0000 0533 START:  MOVEA.L #STRTMSG,A5
000006  6100 0390                     BSR  MESSAGE

00000A  23CF 0000 03A6                MOVE A.L A7,SPSAV
000010  2038 0008                      MOV E.L  $8,D0
000014  7201                           MOV E.L  #1,D1          INCREMENT FOR ADDRESS ON 1ST PASS
000016  3801                           MOV E    D1,D4           INIT AITG-VME NOT FOUND
000018  3801                           MOV E    D1,D4            INIT TPRO-IP NOT FOUND
000022  21FC 0000 006E 0008           MOVE A.L #TRAPISR,$8     ADDRESS OF INTR SERVICE ROUTINE FOR BERR
00002A  227C 00FE FFFF                MOVE A.L #ILLEGAL-1,A1
000030  D3C1                          INCNEXT:ADD. L   D1,A1
000032  1411                          NEXT:      MOVE     #0,D4           FLAG AITG-VME FOUND
000034  3A3C 0000            DT60XX: MOVE    #0,D5           FLAG TPRO-IP FOUND
000038  2E79 0000 03A6               TRAPISR:MOVEA .L SPSAV,A7        POP TRAP ADDR
00003C  8A45                           OR      D5,D5           YES - WAS TPRO-IP DTACK FOUND ?
00003E  66D4                           BNE      NO60XX          NO
000040  66B4                           BNE      INCNEXT         NO
000044  8458                           BRA     DT0A0X
000046  8A45                           OR      D5,D5           YES - WAS TPRO-IP DTACK FOUND ?
000048  66B4                           BNE      NO60XX          NO
00004A  21FC 0000 006E 0008           MOVEA.L #TRAPISR,$8     ADDRESS OF INTR SERVICE ROUTINE FOR BERR
000050  6100 0340                     BSR  MESSAGE
000054  27C 0000 056E               NO60XX:MOVEA.L #NODTACK,A5
000058  6100 03CC                     BSR  MESSAGE
00005E  7200                           MOVE   #0,D1  PREVENT FURTHER ADDR INCR FOR SCOPE LOOP
000060  60D0                           BRA  NEXT
000062  383C 0000               DT0A0X:MOVE    #0,D4     FLAG AITG-VME FOUND
000066  60C8                           BRA  INCNEXT
000068  3A3C 0000            DT60XX:MOVE    #0,D5           FLAG TPRO-IP FOUND
00006C  60C2                           BRA  INCNEXT
00006E  2E79 0000 03A6               TRAPISR:MOVEA.L SPSAV,A7        POP TRAP ADDR
```

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60  ********************************************************** CHECK ID DATA **********************************************************
61  000088 2A7C 0000 05C2 MOVEA.L #IDBEG,A5
62  00008E 6100 0308 BSR MESSAGE
63  000092 323C 03E8 MOVE #1000,D1 LOOP COUNT FOR 1000 CHECKS OF ID DATA
64  000096 27 CC 00FF 6081 IDLOP1 MOVEA.L #PID,A1
65  00009C 247C 0000 041F MOVEA.L #IDCHK,A2
66  0000A2 30C3 000B MOVE #11,D0 CHECK 12 BYTES
67  0000A8 B509 IDLOP2 CMP.B (A1)+,(A2)+
68  0000AC 4A19 TST.B (A1)+ TEST ONLY ODD BYTE ADDRESSES
69  0000AE 51C8 FFF6 DBF D1,IDLOP1 DO 1000 PASSES
70  0000B2 51C9 FFE2 DBF D0,IDLOP2 CHECK 12 BYTES EACH PASS
71  0000B6 6000 0012 BRA IE IF ALL 12 BYTES OK FOR ALL PASSES
72  0000BA 4A21 TST.B -(A1) MOVE ADDRESS BACK TO ERROR ADDRESS
73  0000BC 60EC BRA IESETOK
74  0000C2 6100 02C6 BSR MESSAGE
75  0000C6 4A11 TST.B (A1) LOOP ON BAD ADDRESS
76  0000CA 60FC BRA FATAL
77  0000CB 2A7C 0000 06FA MOVEA.L #ECHOBEG,A5
78  0000D0 6100 0256 BSR MESSAGE
79  0000D4 13FC 00FF 6001 MOVE.B #$1B,IPCMD PUT TPRO-IP IN ECHO MODE
80  0000D8 0839 0000 00FF 6001 BTST.B #BMATIE,IPSTS
81  0000DC 1039 00FF 6001 MOV.B IPSTS,D0
82  0000E0 0C00 00FF 6001 CMP.B #BMATIE,IPSTS
83  0000E4 0000 00FF 6001 CMPI.B #BMATIE,IPSTS
84  0000E8 6000 0012 BRA IE IF ALL 12 BYTES OK FOR ALL PASSES
85  0000EA 6000 000C MOVEA.L #RSTTST,A5 MOVEAIL #IENOSET,A5
86  0000F4 6000 02A2 BSR MESSAGE
87  0000F8 2A7C 0000 0681 IE MOVEA.L #IETST,A5
88  0000FE 6100 020C BSR MESSAGE
89  000102 13FC 00FF 6001 MOVE.B $1B,IPCMD PUT TPRO-IP IN ECHO MODE
90  000106 0839 0000 00FF 6001 BTST.B #BMATIE,IPSTS
91  00010A 6000 000C MOVE.D 1,IPRESET
92  00010E 0839 0006 00FF 6001 BTST.B #BMATIE,IPSTS
93  000110 6700 000C MOVEA.L #RSTTST,A5 MOVEAIL #IENOSET,A5
94  000114 6000 000C MOVE.D 1,IPRESET
95  000118 6700 000C MOVEA.L #RSTTST,A5 MOVEAIL #IENOSET,A5
96  00011C 6000 000C MOVE.D 1,IPRESET
97  00011E 6000 000C MOVEA.L #RSTTST,A5 MOVEAIL #IENOSET,A5
98  000122 6000 000C BRA IESETOK
99  000126 13FC 00FF 6001 MOVE.B D1,IPIFIR PURGE FIFO
100  00012A 0839 0000 00FF 6001 BTST.B #BMATIE,IPSTS
101  00012E 6000 000C MOVEA.L #RSTTST,A5 MOVEAIL #IENOSET,A5
102  000130 6000 000C BRA IESETOK
103  000134 2A7C 0000 077C ECHRTO:ADDI.B 1,D1 ECHTST MOVEA.L #ECHOBEG,A5
104  00013A 6100 0225 BSR MESSAGE
105  00013E 13FC 00FF 6003 MOVE.B $1B,IPCMD PUT TPRO-IP IN ECHO MODE
106  000142 0839 0000 00FF 6003 BTST.B #BMATIE,IPSTS
107  000146 6000 000C BRA IESETOK
108  00014A 4A39 00FF 6003 TST.B IPFIFO PURGE 1B
109  00014E 343C 0014 MOVE #20,D2 DO 20 LOOPS OF ALL VALUES
110  000152 13FC 00FF 6003 ECHTST:ADDI.B 1,D1 ECHTST MOVEA.L #ECHOBEG,A5
111  000158 6100 015A BSR WT100
112  00015D 30C3 07D0 MOVE #2000,D0
113  000161 6010 01D2 BRA WTECHOL WAIT FOR “1B” TO ECHO
114  000165 6100 001B4 MOVE.B $1B,IPCMD IF 1-255 WRITTEN TO CMD PORT
115  000169 60EC BSR CMDLOP
116  00016D 131C 00FF 6003 MOVE.B D1,IPCMD
117  000171 6000 000E BEQ WTECHOL
118  000175 6100 02E BRA ECHTST
119  000179 6000 000E BEQ WTECHOL
120  00017D 6100 02E BRA ECHTST

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<td>00017E 0839 0000 00FF 6001</td>
<td>BTST.B #0,IPSTS BYTE SHOULD BE ECHOED TO FIFO NOW</td>
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<td>118</td>
<td>000186 6700 0016</td>
<td>BEQ NOECHER IF NOT, REPORT NO ECHO &amp; TRY AGAIN</td>
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<td>119</td>
<td>00018A 1639 00FF 6003</td>
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<td>120</td>
<td>000190 B203</td>
<td>CMP.B D3,D1</td>
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<td>121</td>
<td>000192 67E2</td>
<td>BEQ WT100</td>
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<tr>
<td>122</td>
<td>000194 2A7C 0000 07BE</td>
<td>BADECH MOVE.AL #ECHOBAD,A5</td>
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<tr>
<td>123</td>
<td>000196 6100 01F6</td>
<td>BSR FATAL</td>
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<td>124</td>
<td>000198 2A7C 0000 07F2</td>
<td>MOVEA.L #ECHOBAD,A5</td>
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<td>125</td>
<td>00019A 6100 01F2</td>
<td>BSR MESSAGE</td>
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<td>00019C 32C0 0000</td>
<td>TRY 0-255 VECTOR PATTERN</td>
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<td>VECLOP MOVE.B D1,IPVEC WRITE TO INT VECTOR REG</td>
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<td>128</td>
<td>0001A2 6100 00F6</td>
<td>BSR WT100</td>
</tr>
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<td>129</td>
<td>0001A4 6000 0008</td>
<td>BRA INT0TST</td>
</tr>
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<td>130</td>
<td>0001A6 2A7C 0000 082E</td>
<td>MOVEA.L #ECHOOK,A5</td>
</tr>
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<td>131</td>
<td>0001A8 6100 01F2</td>
<td>BSR MESSAGE</td>
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<td>132</td>
<td>0001AA 0601 0001</td>
<td>ADDLB #1,D1 ALL DONE ?</td>
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<tr>
<td>133</td>
<td>0001AC 6600 0012</td>
<td>BNE BADVECT</td>
</tr>
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<td>134</td>
<td>0001AE 0601 0001</td>
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</tr>
<tr>
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<td>VECLOP MOVE.B D1,IPVEC WRITE TO INT VECTOR REG</td>
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<td>138</td>
<td>0001A6 2A7C 0000 082E</td>
<td>MOVEA.L #ECHOOK,A5</td>
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<td>VECLOP MOVE.B D1,IPVEC WRITE TO INT VECTOR REG</td>
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<td>144</td>
<td>0001A2 6100 00F6</td>
<td>BSR WT100</td>
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<td>0001A4 6000 0008</td>
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<td>146</td>
<td>0001A6 2A7C 0000 082E</td>
<td>MOVEA.L #ECHOOK,A5</td>
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<td>0001A8 6100 01F2</td>
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<tr>
<td>152</td>
<td>0001A2 6100 00F6</td>
<td>BSR WT100</td>
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<td>0001A4 6000 0008</td>
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<td>154</td>
<td>0001A6 2A7C 0000 082E</td>
<td>MOVEA.L #ECHOOK,A5</td>
</tr>
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<td>155</td>
<td>0001A8 6100 01F2</td>
<td>BSR MESSAGE</td>
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<tr>
<td>156</td>
<td>0001AA 0601 0001</td>
<td>ADDLB #1,D1 ALL DONE ?</td>
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<td>0001AC 6600 0012</td>
<td>BNE BADVECT</td>
</tr>
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<td>158</td>
<td>0001AE 0601 0001</td>
<td>ADDLB #1,D1 ALL DONE ?</td>
</tr>
<tr>
<td>159</td>
<td>0001A0 13C1 00FF 6005</td>
<td>VECLOP MOVE.B D1,IPVEC WRITE TO INT VECTOR REG</td>
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<tr>
<td>160</td>
<td>0001A2 6100 00F6</td>
<td>BSR WT100</td>
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<tr>
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<td>0001A4 6000 0008</td>
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<tr>
<td>162</td>
<td>0001A6 2A7C 0000 082E</td>
<td>MOVEA.L #ECHOOK,A5</td>
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<td>MOVEA.L #ECHOOK,A5</td>
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<td>0001A8 6100 01F2</td>
<td>BSR MESSAGE</td>
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<tr>
<td>172</td>
<td>0001AA 0601 0001</td>
<td>ADDLB #1,D1 ALL DONE ?</td>
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<tr>
<td>173</td>
<td>0001AC 6600 0012</td>
<td>BNE BADVECT</td>
</tr>
</tbody>
</table>

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9-12 Synchronizable Timecode Generator User Manual
Synchronizable Timecode Generator User Manual

...
Title: IPTST2.001 INIC TPRO-IP VME BUS LATCHED VS FIFO DELTA

Note: For this demo, host is a Xycom XVM-E 600 (10 MHz 68000)

00FF 6001 IPS TS EQU SFF6001
0000 0000 BSTS OR EQU 0 BIT0: FIFO NOT EMPTY READ ONLY.
00FF 6003 IPFF O EQU SFF6003 FIFO DATA PORT (READ ONLY)
00FF 6009 IPTAG EQU SFF6009 SIMULATED EXTERNAL EVENT PORT. WRITE ONLY
00FF 600D IPFIF R EQU SFF600D FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
00FF 6008 IPLO EQU SFF6008 A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
00FF 600E I PFI E EQU SFF600E A16 BUS WINDOW FOR MVME133+BASE+E OFFSET

000000 247C 0000 0102 START: MOVEA.L #STRTMSG,A5
000006 6100 00D0 BSR MESSAGE

******** CHECK SECONDS 0-59 PARALLEL=FIFO TIME ********
00000A 13C0 00FF 600D CHKSEC MOVE.B D0,IPFIFR CLEAR FIFO OF IRQ0 TEST DATA
000010 6100 0076 BSR TAGNPAR GET TIME TAG FIFO DATA & PARALLEL TIME
000014 247C 0000 00FA MOVE.L #HISAV+8,A0
00001A 247C 0000 0102 MOVE.L #DELTA+8,A2
000020 023C 0000 AND I.B #0,CCR
000024 323C 0007 MOV E #7,D1 DO 8 BYTES
000028 1520 DELTLOP MOVE .B -(A0),-(A2) DELTA = PARALLEL - FIFO
00002A 4A1A TST.B -(A2)+ SBCD NEEDS AUTODEC MODE
00002C 8509 SBC D -(A1),-(A2)
000032 6100 0042 BSR WT100 LIMIT MAX EVENT RATE
000036 3239 00FF 6001 WT100L: BTST. B #1,IPSTS LIMITS LOOP SPEED TO I/O SPEED
00003C 67C8 BEQ CHKSEC
000042 247C 0000 0141 MOVEA.L #ASCBUF,A5 CONVERT FIFO, PAR, DELT TO ASCII
000048 233C 0017 MOV E #24-1,D1 LOOP COUNT FOR 24 BYTES
00004C 3407 ASCLOP MOVE .B (A1)+,D7 GET 2 NIBBLES
000050 E84F LSR #4,D7 RIGHT JUSTIFY HI ORDER NIBBLE
000052 0207 000F ANDL B #50F,D7
000056 0603 0030 ADDLB #"0",D7
00005A 1AC7 MOVEB D7,(A5)+ MOVEA.L #ASCBUF,A5
00005C 0202 000F ANDLB #50F,D2
000060 0602 0030 ADDLB #"0",D2
000064 1AC2 MOVE.B D2,(A5)+
000066 51C9 FFE8 DBF D1,ASCLOP
00006A 247C 0000 0141 MOVEA.L #ASCBUF,A5
000070 6100 0066 BSR MESSAGE:
000074 6094 BRA CHKSEC
000076 303C 00FF WT100: MOVE #5FF.D0
00007A 0839 0001 00FF 6001 WT100L: BSTS.B #1,IPSTS LIMITS LOOP SPEED TO I/O SPEED
000082 51C8 FFE6 DBF D0,WT100L
000086 4E75 WRTS: RTS

********** SUBROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6 *****
000088 13FC 0000 00FF 6009 TASNPAR MOVE.B #0,IPTAG TRIGGER EVENT BCD TIME REPORT
000090 33F9 00FF 6008 0000 MOVE IPLO,HISAV+6
000093 33F9 00FF 600A 0000 MOVE IPLO+2,HISAV+4
0000A3 33F9 00FF 600C 0000 MOVE IPLO+4,HISAV+2
0000AE 33F9 00FF 600E 0000 MOVE IPLO+6,HISAV
Lines Assembled : 78      Assembly Errors : 0
00FF 6008
IPLO EQU SFF6008  A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
8 000000 2A7C 0000 00EA
START: MOVEA. L #STRTMSG,A5
9 000006 6100 00B8
BSR MESSAGE
10
***********CHECK SECONDS 0-59 PARALLEL=FIFO TIME***********
11 00000A 33F9 00FF 6008 0000
CHKSEC: MOVE IPLO,EVTDAT+6
12 000014 33F9 00FF 600A 0000
MOVE IPLO+2,EVTDAT+4
13 000018 33F9 00FF 600C 0000
MOVE IPLO+4,EVTDAT+2
14 00001C 33F9 00FF 600E 0000
MOVE IPLO+6,EVTDAT
15 000020 33F9 00FF 6008 0000
MOVE IPLO,HISAV+6
16 000024 33F9 00FF 600A 0000
MOVE IPLO+2,HISAV+4
17 000028 33F9 00FF 600C 0000
MOVE IPLO+4,HISAV+2
18 00002C 33F9 00FF 600E 0000
MOVE IPLO+6,HISAV
19 000030 227C 0000 00DA
MOVEA. L #EVTDAT+8,A1
20 000036 207C 0000 00E2
MOVEA. L #HISAV+8,A0
21 000042 247C 0000 00EA
MOVEA. L #DELTA+8,A2
22 000048 023C 0000
ANDI. B  #0,CCR
23 00004C 323C 0007
MOVE #7,D1
DO 8 BYTES
24 000050 1520
DELTLO P MOVE. B  -(A0),-(A2) DELTA = PARALLEL - FIFO
25 000052 4A1A
TST.B   (A2)+ SBCD NEEDS AUTODEC MODE
26 000054 8509
SBCD  -(A1),-(A2)
27 000058 51C9 FFF8
DBF   D1,DELTLOP
28 00005C 3239 00FF 6008 0000
MOVE DELTA+6,D1
29 000060 51C9 0000 00E8
DBF   D1,DELTLOP
30 000064 3239 00FF 600A 0000
MOVE DELTA+4,D1
31 000068 51C9 0000 00E8
DBF   D1,DELTLOP
32 00006C 3239 00FF 600C 0000
MOVE DELTA+2,D1
33 000070 51C9 FF4C
DBF   D1,DELTLOP
34 000074 3239 00FF 600E 0000
MOVE DELTA,D1
35 000078 2A7C 0000 0119
MOVEA. L #ASCBUF,A5 CONVERT FIFO, PAR, DELT TO ASCII
36 000080 6100 0006
BSR MESSAGE
37 000084 6000 FF4C
BRA CHKSEC
38 000088 4D 45 41 53 55 52
STRTMSG:ASCII MEASURE 2 PARALLEL TIMES, DISPLAY IF BIG DELTA
39 000090 00
BYTE 0
40 000091 30 30 30 30 30 30
ASCBUF: ASCII 000000000000000000000000000000000000000000000000
Spectracom Corporation

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******************************************************************************
* TITLE IPTST4.001 *TNOV4+ ICK TPRO-IP VME BUS DISPLAY FIFO & PAR TIME & DELTA
* NOTE: FOR THIS DEMO, HOST IS A XYCOM XVME-600 (10 MHZ 68000)
******************************************************************************

7 00FF 6001      IPSTS EQU $FF6001
8 0000 0000      BSTSOR EQU 0  BIT0: FIFO NOT EMPTY  READ ONLY.
9 00FF 6003      IPFFO EQU $FF6003  FIFO DATA PORT (READ ONLY)
10 00FF 6009      IPTAG EQU $FF6009D  FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
11 00FF 6008      IPLO EQU $FF6008  A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
12 00FF 600E      IPHI EQU $FF600E  A16 BUS WINDOW FOR MVME133+BASE+E OFFSET

13 000000 2A7C 0000 0106 START:   MOVEA.L #S TRTMSG,A5
14                        6100 00D4                     BSR     MESSAGE
15 17 00000A 13C0 00FF 6001CHKSEC  MOVE.B D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
16 17 00000D 007A 00FF 600DCHKSEC  MOVEA.L #HISA V+8,A0
17 17 000011 2A7C 0000 00FE       MOVEA.L #HISA V+8,A2
18 17 000016 023C 0000 0072 0104       MOVE    DELTA +6,D1
19 17 00001B 1E19                 DELTLOP     MOVE.B  -(A0),-(A2)     DELTA = PARALLEL - FIFO
20 17 00001D 4A1D                          TST. B   (A2)+           SBCD NEEDS AUTODEC MODE
21 17 00001F 8509                          SBCD     -(A1),-(A2)
22 17 000021 51C9 FFF8            DBF     D1,DELTLOP
23 17 000025 6100 0046                     BSR     WT100           LIMIT MAX EVENT RATE
24 17 000029 3239 0000 0104       MOVE    DELTA+6,D1
25 17 00002D 00FF 6009 0000 0145  MOVEA.L #ASCBUF,A5   CONVERT FIFO, PAR, DELT TO ASCII
26 17 000031 33F9 00FF 6008 0000  MOVE    IPLO, HISAV+6
27 17 000035 33F9 00FF 600A 0000  MOVE    IPLO+2,HISAV+4
28 17 000039 33F9 00FF 600C 0000  MOVE    IPLO+4,HISAV+2
29 17 00003D 33F9 00FF 600E 0000  MOVE    IPLO+6,HISAV+0
30 17 00003F 6090                          BRA     CHKSEC
31 17 000043 0839 0001 00FF 6001  WT100L: BTST. B  #1,IPSTS         LIMITS LOOP SPEED TO I/O SPEED
32 17 000047 51C8 00FF 600F 0000  MOVE    D1,ASCLOP
33 17 00004B 4A1D                          TST. B   (A5)+           LEAVE A SPACE
34 17 00004D 51C8 FFED                          DBF     D0,ASCLOP
35 17 00004F 51C8 FFED                          DBF     D0,ASCLOP
36 17 000051 1AC7                          MOVEA.L #ASCBUF,A5
37 17 000053 6000 007A 00FF 6001  WT100L: BTST. B  #1,IPSTS         LIMITS LOOP SPEED TO I/O SPEED
38 17 000057 0602 0030 00FF 600F  MOVEA.L #ASCBUF,A5
39 17 00005B 0602 0030 00FF 600F  ADDI .B  #$0F, D0
40 17 00005D 0602 0030 00FF 600F  ADDI .B  #$0F, D0
41 17 00005F 0602 0030 00FF 600F  ADDI .B  #$0F, D0
42 17 000061 0602 0030 00FF 600F  ADDI .B  #$0F, D0
43 17 000063 0602 0030 00FF 600F  ADDI .B  #$0F, D0
44 17 000065 0602 0030 00FF 600F  ADDI .B  #$0F, D0
45 17 000067 0602 0030 00FF 600F  ADDI .B  #$0F, D0
46 17 000069 0602 0030 00FF 600F  ADDI .B  #$0F, D0
47 17 00006B 0602 0030 00FF 600F  ADDI .B  #$0F, D0
48 17 00006D 0602 0030 00FF 600F  ADDI .B  #$0F, D0
49 17 00006F 0602 0030 00FF 600F  ADDI .B  #$0F, D0
50 17 000071 0602 0030 00FF 600F  ADDI .B  #$0F, D0
51 17 000073 0602 0030 00FF 600F  ADDI .B  #$0F, D0
52 17 000075 0602 0030 00FF 600F  ADDI .B  #$0F, D0
53 17 000077 0602 0030 00FF 600F  ADDI .B  #$0F, D0
54 17 000079 0602 0030 00FF 600F  ADDI .B  #$0F, D0
55 17 00007B 0602 0030 00FF 600F  ADDI .B  #$0F, D0
56 17 00007D 0602 0030 00FF 600F  ADDI .B  #$0F, D0

******************************************************************************
* SUBROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6 *****
******************************************************************************

30 000000 13C0 00FF 6001CHKSEC  MOVE.B D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
31 000000 13C0 00FF 6001CHKSEC  MOVE.B D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
32 000000 13C0 00FF 6001CHKSEC  MOVE.B D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
33 000000 13C0 00FF 6001CHKSEC  MOVE.B D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
34 000000 13C0 00FF 6001CHKSEC  MOVE.B D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
00F6
57 0000BC 22C 0000 00EC MOVEA.L #EVTDAT-2,A1
58 0000C2 323C 0009 MOVE #9,D1
59 0000C6 0839 0000 00FF 6001 WTFIFA: BTST.B #0,IPSTS READ 10 BYTES OF FIFO DATA
60 0000CE 67F6 BEQ WTFIFA
61 0000D0 12F9 00FF 6003 MOVE.B #IFSIFO,(A1)+ READ WITHOUT MESSING UP A REGISTER
62 0000D6 51C9 FFEE DBF D1,WTFIFA
63 0000DA 4E75 RTS
64 0000DC 3C4D MESSAGE: MOVE A5,A6
65 0000DE 4A1E MSGEND: TST.B (A6)+ FIND END OF MESSAGE
66 0000E0 66FC BNE MSGEND
67 0000E2 4A26 TST.B -(A6)
68 0000E4 4F75 TRAP #15
69 0000E6 0002 DW $2
70 0000EA 0000 0000 LWOR D 0
71 0000EE 0000 0000 0000 0000 EVTDAT: LWORD 0
72 0000F6 0000 0000 0000 0000 HISAV: LWORD 0, 0 SEC,FRAC
73 0000FE 0000 0000 0000 0000 DELTA: LWORD 0, 0
74 000106 53 49 4D 20 45 58 STRTMSG: ASCII SIM EXT EVT, READ PARALLEL, DISPLAY BIG DELTA PARALLEL-EXT EVT
75 00010C 00 00 00 00 00 ASCBUF: ASCII 00000000000000 00000000000000 00000000000000 00000000000000
76 000144 00 .BYTE 0
77 000177 00 .BYTE 0
78 000178 END

Lines Assembled: 79 Assembly Errors: 0
**INTERRUPT SERVICE ROUTINE**

**TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6**

**DISABLING FIFO OR INTERRUPTS WHILE READING FIFO**

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**INTERRUPT SERVICE ROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6**

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**INTERRUPT SERVICE ROUTINE**

**TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6**

**DISABLING FIFO OR INTERRUPTS WHILE READING FIFO**
59 0000C0 33F9 00FF 600A 0000
   001A
60 0000CA 33F9 00FF 600C 0000
   0018
61 0000D4 33F9 00FF 600E 0000
   0016
62 0000DE 227C 0000 010C
63 0000E4 323C 0009
64 0000E8 0839 0000 00FF 6001
65 0000F0 67F6
66 0000F2 12F9 00FF 6003
67 0000F8 51C9 FFEF
68 0000FC 13FC 0090 00FF 6001
69 000104 4CDF 0202
70 000108 4E73
71 00010A 0000 0000
72 00010E 0000 0000 0000 0000
73 000116 0000 0000 0000 0000
74 00011E 0000 0000 0000 0000
75 000126 00
76 000127 30 30 30 30 30
77 000159 00
78 00015A

MOVE   IPLO+2,HISAV+4
MOVE   IPLO+4,HISAV+2
MOVE   IPLO+6,HISAV

MOVEA.L #EVTDAT-2,A1
MOVE   #9,D1       READ 10 BYTES OF FIFO DATA
BEQ WTFIFA
MOV.E  IPFIFO,(A1)+     READ WITHOUT MESSING UP A REGISTER
DBF   D1,WTFIFA
MOVE.B  #1.SHL.BORIE+1.SHL.BEXTENB,IPSTS    REENABLE FIFO NOT EMPTY INTR
MOVEM.L (A7)+.D1/A1    RESTORE A0 AND D0

WTFIFA: BTST.B   #0.IPSTS FOR EACH BYTE, CHECK FOR READY. **IMPORTANT!**
BEQ WTHIFA
MOV.E.B  #1.SHL.BORIE+1.SHL.BEXTENB,IPSTS    REENABLE FIFO NOT EMPTY INTR

Lines Assembled :  78     Assembly Errors :  0
10 Driver Support

Please contact your sales representative for information about Spectracom’s bus-level timing board driver support for a variety of other platforms. You may also visit our website at www.spectracomcorp.com to download datasheets and manuals.
# REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision Level</th>
<th>ECN Number</th>
<th>Description</th>
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<tbody>
<tr>
<td>A</td>
<td>2187</td>
<td>First conversion of legacy KSI documentation (level 4.1).</td>
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