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The Global Leader in Resilient PNT

Patented Smart GRClok-1500

Auto-Adaptive GPS/GNSS SmarTiming+® Technology

Optional SMA connector for GPS/ GNSS antenna kit when GPS/ GNSS receiver is embedded

INSIDE SMARTIMING+ TECHNOLOGY

LEAD FREE RoHS COMPLIANT

Applications

Telecom | Navigation | Broadcast
Defense | Instrument

KEY FEATURES

- Ultra low aging in hold-over mode : < 3E-11/ month
- Frequency offset over temp. range : ± 1E-10
- Optionally integrated GPS/GNSS receiver
  - SMA input connector : 1575.42 MHz from GPS/GNSS antenna
  - NMEA 0183 messages on RS232 : Standard $GPRMC and $GPZDA
- Short-term stability : 1E-12 @ 100s
- Industry's first SmarTiming+® technology
  - Input REF locking resolution : 1 ns
  - Input REF disciplining/filtering/controlling : Auto adaptive
    - *Smart loop time constant* *: 1000 - 100,000 sec*
    - *E1/T1 jitter & wander* *: ITU-T G.823/824*
  - Input REF locking mode (user settable) : Sync[a] or Track[b]
  - Output frequency accuracy/stability
    - *PRS(c)/Stratum 1 locked* *: 1E-12, typical*
    - *Holdover (No PRS[c]/GPS)* *: <3E-11/month*
  - Output time accuracy/stability
    - *GPS locked* *: <50ns*
    - *Holdover (no PRS[c]/GPS)* *: <2µs/48 hr or <1µs/24 hr*
  - Standards compliance
    - *PRS[c] locked/unlocked* *: ANSI T1.101, Stratum 1 / 2, GR-1244, ITU-T G.811/G.812, PRC, Type II CDMA IS-95, UMTS 3GPPS 25.104*
- Small volume : 28 in^3 (5x3.74x1.5" / 128x95x38.1mm)
- Single power supply voltage : 12V or 24V
- RS232 standard interface : Control & monitoring commands, 9600 b/s

Notes

(a) Phase alignment (Output signal phase aligned to the REF/Reference signal)
(b) Frequency alignment (Output signal frequency aligned to the REF/Reference signal)
(c) PRS: Primary Reference Source such as GPS / GNSS, Cesium, and Maser

SPECIFICATIONS

ELECTRICAL

Spec	Smart GRClok-1500			
Type	**Standard**	**Options**		
RFOUT Frequency	10 MHz	Integrated synthesizer **(order code: xM)** x : 2.048M,4.096M,10.23M etc		
Frequency Change Operating temperature range (Thermal chamber with air flow)	+-1E-10 -10°C to +55°C	±2E-10 ±1E-10	-32 to 60°C **(order code: E)** 0 to 55°C **(order code: LP)**	
Frequency Accuracy @ Shipment	< 5E-11 (+25°C), typical			
Aging (After 3 months of continuous operation)	< 5E-11 / month (typical: 3E-11 / month)	< 3E-11 / month or 2E-10 / year **(order code: A)** (typical: ±1E-11 / month)		
Short Term Stability 1s 10s 100s	 2E-11 8E-12 3E-12	**(order code: S)** 1E-11 3E-12 1E-12		
Phase Noise (dBc/Hz) (RFOUT 10 MHz) 1 Hz 10 Hz 100 Hz 1k Hz 10K Hz	 -75 -95 -125 -145 -150			
Frequency Retrace Off/On (In stable temperature, gravity, pressure & magnetic field conditions)	 < 5E-11 24 hr / 1 hr			
Warm-up Time @ +25°C Frequency stability	12 min 5E-10	Lock < 7 min **(order code: F)**	Lock < 5min **(order code: FE)**	25 min 5E-10 **(order code: LP)**
Analog Frequency Adjustment Tolerance [An external voltage (0-5 VDC) can be applied to pin 6 (FA). The cursor pin of a 10 kΩ variable resistor placed between pin 7 and GND can provide this voltage. If not used, pin 6 must be floating]	5×10^{-9} ±20%			
Digital Frequency Adjustment Internal crystal oscillator freq. Resolution (Through RS-232 commands)	±1.67E-8 10MHz 5.12E-13			
RFOUT Output level Output impedance Harmonics Spurious f_o ± 100kHz	Sine wave 0.5 Vrms (± 10% / 50Ω) 50 Ω ±20% < -40dBc < -80dBc	With **xM** option: CMOS 0-5V (>20 mA sink/ source)	Sine wave 10dBm (±10% / 50Ω) **(order code: 10DBM)**	
Communication Interface Protocol speed	RS-232 control & monitoring (see commands below) 9600, n, 8, 1			
Supply Voltage (DC)	24V (20 to 32 V)	12V (11.2 to 16 V) **(order code: 12V)**		
Max Power Supply Ripple	< 50 mV peak to peak (from 1Hz to 1 MHz frequency band)			
Input Power Warm up @+25°C (typical) 0°C +25°C +60°C	<30W @12V or <38W @ 24V Typ. 20 W Typ. 15 W Typ. 10 W	**with the following options:** **(F/E)** <40 W (24V only)	**(FE)** <50 W (24V only)	**(LP)** <24W
		Option GPS : +2W		
Conformal coating	None	Included **(order code: CC)**		
Reverse Voltage Protection	< -40V (up to -40V on power input / no damage)			
Electrical Protection power +24V (12V) RF output TxD output RxD input Frequency adjust input Lock indicator	 An internal diode protects against reverse polarity connection ESD and short-cut protected ESD and short-cut protected ESD protected ESD protected Over current protected			
Lock Indicator (pin 4) L = open collector B = TTL locked unlocked	**Standard** Open Closed	**Option LR** Closed Open	**Option B** < 0.4V 5V	**Option BR** 5V < 0.4V

INTEGRATED GPS/GNSS RECEIVER WITH SMARTIMING+® DISCIPLINING TECHNOLOGY

Spec	Smart GRClok-1500		
Type	**Standard**	**Options**	
Integrated GPS/GNSS Receiver	Not applicable	**(order code : GPS)**	
GPS/GNSS Antenna Kit Input Cable connector Active antenna voltage	Not applicable	**(order code : PA)** SMA 5V Patch antenna 6 m/19.7' Included	
GPS/GNSS Antenna Kit Antenna type Lightning surge protector Cable length	Not applicable	**(order code: PA)** Patch antenna Not applicable ≥5 m/16.4'	**(order code: RA)** Rooftop antenna Included **(order code:CA)** 5+15m/16.4'+49'
Antenna mounting bracket	Not applicable	**(order code: BRA)**	
Input PPSREF Level Reference types Disciplining & filtering Disciplining mode Architecture Model	CMOS 0-5V or 0-3.3V rising edge GPS/GNSS/E1/T1/Cesium/Maser Auto-adaptive thru SmarTiming+® technology (request White Paper) Sync (phase alignment) or Track (frequency alignment) See Operational Principles below	Not applicable	
GPS/GNSS Receiver Control T-RAIM @ startup time Position hold @ startup time	Request GPS/GNSS iSync+ Connectivity AppNotes Auto-configured, if supported by receiver Auto-configured, if supported by receiver	Auto-configured Auto-configured	
PPSOUT Output Output Level Pulse Width or duty cycle (PW)	1PPS CMOS 0-5V (±20 mA sink/source) User settable, 0 to 1s in 66ns/step		
PPSOUT to PPSREF Sync Error Conditions (Sync Mode)	< 50 ns No PPSRef noise, ± 1°C temp fluctuations		
PPSOUT to PPSREF (DE) Programmable delay (Track mode)	0 to 1s in 66ns/step		
PPSOUT Holdover Time Stability Temperature window (After learning phase > 10_T)	< 1µs / 24 hr < 7µs / 1 week Within ±2°C	< 3µs / 24 hr Within 20°C	< 7µs / 24 hr Within 40°C
Smart Loop Time Constant Phase/Frequency User settable	Auto-adaptive 1,000 to 100,000 sec Sync/Trak mode RS-232 command interface		
Communication Interface GPS/GNSS Protocol speed	RS-232 control & monitoring (see commands below) 9600, n, 8, 1		

ENVIRONMENTAL

Spec	Smart GRClok-1500
Magnetic Field Sensitivity	< 2E-11 / Gauss (< 1E-10 / Gauss in longitudinal axis)
Storage Temperature	- 55°C to + 85°C
Humidity	GR-CORE-63, Section 5.1.2
Operating Vibration	GR-CORE-63, Section 5.4.2 Random and Sinusoidal MIL-PRF-28800F, Class 3, 4
Shock	Survival: 40g / 11ms
Helium concentration sensitivity	< 1E-10 per ppm of Helium concentration change
G-Tip-Over Test	< 2E-10 / g in worst axis

PHYSICAL

Spec	Smart GRClok-1500	
Size (L x W x H)	5x3.74x1.5" / 128x95x38.1mm	
Weight	500g (17.64oz)	
Mounting & Mechanical Layout Screw fixture type (6 pieces)	see drawings below UNC-4-40	Not applicable M3 **(order code: M3)**
Connectors Male D-sub 25 pins SMA RFOUT coaxial SMA GPS/GNSS Input coaxial	see pin-out & drawing data below 10MHz GPS/GNSS antenna kit	
Warranty	Electronics : 1 year; Lamp & cell : 20 years	

ORDERING INSTRUCTIONS

GRClok-1500 / 10M / 12V / xx

Type — Frequency — Supply voltage — Options (GPS/S/RA/Etc)

KEY OPERATIONAL PRINCIPLES

The smart GRClok-1500 uses SmarTiming+® technology. It auto-adaptively locks multi-vendor Stratum-1 references such as GPS, GNSS, Cesium, LORAN-C, CDMA and E1/T1 at industry's first 1ns resolution for the highest performance level, and generates a perfectly aligned 1PPS output signal (PPSOUT) and time of day (TOD) information.

As illustrated in Fig. 1 below, the smart GRClok-1500 has two basic modes of operation: "Track" and "Sync". "Track" is used for frequency alignment while "Sync" is used for phase alignment applications.

In "Track" mode, the smart GRClok-1500 uses an external PPS reference (PPSREF) to align the frequency of the GRClok-1500. The frequency alignment is computed by an internal phase-time error signal that is generated by an internal PPS signal (PPSINT), which measures the signal at 1 ns resolution through its SmarTiming+® technology. The PPSINT then aligns the PPSREF phase.

In the "Sync" mode, the smart GRClok-1500 phase aligns the PPSOUT to the PPSREF with the PPSINT reference signal, which uses SmarTiming+® algorithm to 1) compare the PPSOUT and PPSREF signals at 1ns resolution within a +/-500ns dynamic range and 2) auto-adaptively align them.

The smart GRClok-1500 has also the capability to dynamically analyze the stability of the PPSREF signal through the excellent mid-term frequency stability of the Rubidium technology. Thus, the 1PPS reference of a Stratum-1 source such as GPS can be directly fed to smart GRClok-1500 without specific analysis of the internal optimization parameters of the GPS engine - i.e., number of satellites in view, signal to noise ratio, etc.

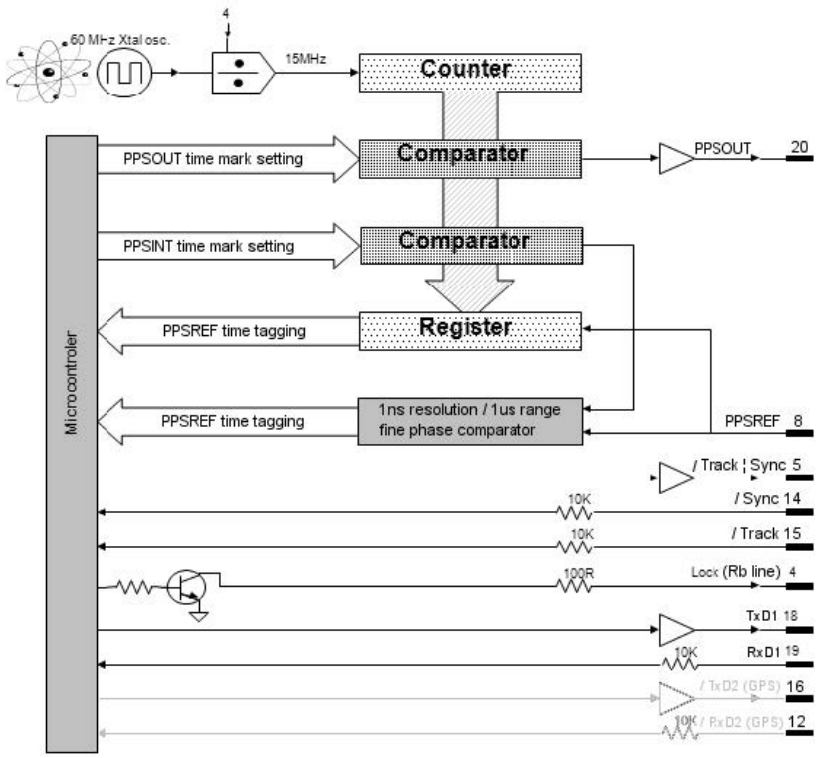


Figure.1: SmarTiming+® Control Block Diagram

As illustrated in Fig. 2 below, the "Track" mode aligns the PPSINT to the PPSREF within 66.6ns. After about 1OT, the PPSINT is perfectly aligned to the PPSREF.

The smart GRClok-1500 is also capable to perfectly align the PPSOUT to the PPSREF or to adjust the PPSOUT from 0-1s with a 66.6ns resolution. This time adjustment can be programmed through the RS232 interface. After a descending edge of the "Sync" signal, the PPSOUT will be aligned to the PPSREF (see figure 2).

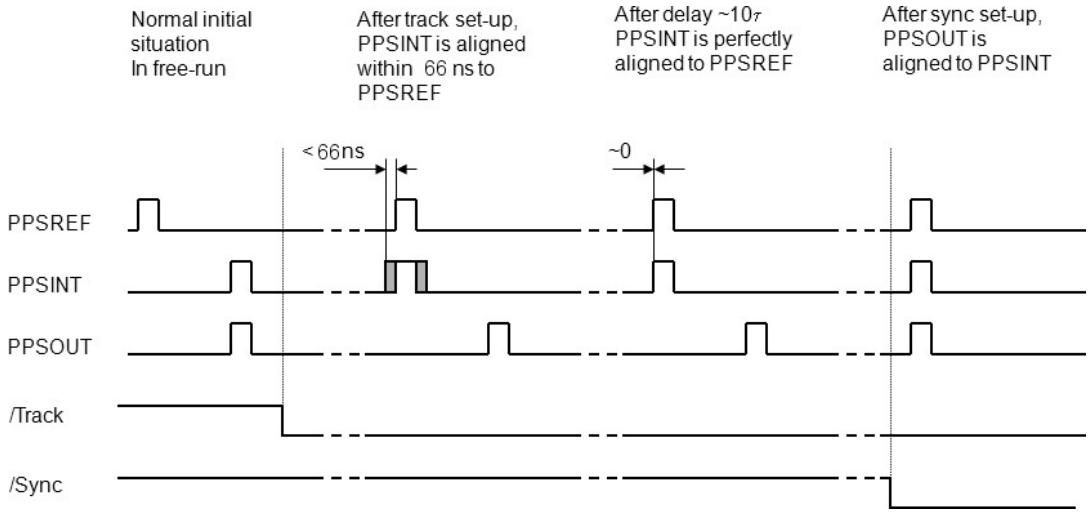


Figure 2 : "Track" & "Sync" Mode

STANDARD RS-232 CONTROL & MONITORING COMMANDS

Frequency Adjustment & Monitoring Functions

The operating and monitoring parameters of the GRClok-1500 are accessible for read and write operations through the serial RS-232 port (9600 bits/sec., no parity, 1 start bit, 8 data bits, 1 stop bit).

There are 2 basics commands, which are M, Cxxxx

M<CR><LF>: monitors the basic internal signals of the atomic clock.

The returned answer looks like

HH GG FF EE DD CC BB AA <CR> <LF>

Where each returned byte is an ASCII coded hexadecimal value, separated by a <Space> character. All parameters are coded at full scale.

HH: Read-back of the user provided frequency adjustment voltage on pin 6 (0 to 5V)
GG: reserved
FF: peak voltage of Rb-signal (0 to 5V)
EE: DC-Voltage of the photocell (5V to 0V)
DD: varactor control voltage (0 to 5V)
CC: Rb-lamp heating current (Imax to 0)
BB: Rb-cell heating current (Imax to 0)
AA: reserved

Cxxxx<CR><LF>: output frequency adjustment through the synthesizer, by steps of 5.12 x 10^{-13} , where xxxx is a signed 16 bits word in hexa coded ASCII. This value is automatically stored in a EEPROM as last frequency which is applied after RESET or power-ON operation.

In Track mode this correction is not in use. The function FCsddddd do the same. But the data format is different.

Timing & Locking Control Functions

Using the same data interface, the smart GRClok-1500 models can accept the following basic ASCII commands: Data is in decimal ASCII code.

Command name	Syntax command	Data field (if any)	Response syntax	Response data (if any)
Identification	**ID**<CR><LF>	-	**SPTLNR**-aaa/rr/s.ss <CR><LF>	aaa: 001. rr: revision number s.ss: software version
Serial number	**SN**<CR><LF>	-	xxxxxx<CR><LF>	xxxxxx : 6 digits serial nbr
Status	**ST**<CR><LF>	-	**s**<CR><LF>	s:Status s=0 :warming up or no light s=1 :tracking set-up s=2 :track to PPSREF s=3 :synch to PPSREF s=4 :Free Run. Track OFF s=5 :FR. PPSREF unstable s=6 :FR. No PPSREF s=7 : FREEZE s=8 :factory used s=9 :searching Rb line
Beat a message on the serial port once per second. Except BT8, BT9.	**BT**x<CR><LF>	x=0 : Stop beat x=1 : Effective Time interval PPSOUT vs PPSREF x=2 : Phase comparator x=3 : Both x=1 & x=2 x=4 : Beat Time of day x=5 : Beat status x=6 : Beat <CR><LF> x=7 : Beat Date, Time, Status x=8 : Spec. PPSREF tagging x=9 : Special GPS message x=A : Beat NMEA $PTNTA, x=B : Beat NMEA $PTNTS,B, x=R : Beat NMEA $GPRMC,.. x=Z : Beat NMEA $GPZDA,..	Various, see Manual	Various, see Manual
View PPSRef Sigma	**VS**<CR><LF>		ddd.d<CR><LF>	ddd.d : Sigma of PPSRef in ns. In tracking, Status 2, 3.
View Time constant	**VT**<CR><LF>		dddddd<CR><LF>	dddddd : Loop time constant now in use, in second.
Set Tracking PPSINT - PSSREF	**TR**x<CR><LF>	x=0 : set tracking state : OFF x=1 : set tracking state : ON x=?: interrogation	x<CR><LF>	x:Tracking state x=0 :tracking state OFF x=1 : tracking state ON
Set Synchronisation PPSOUT – PPSINT	**SY**x<CR><LF>	x=0 : set synch. state : OFF x=1 :set synch. state : ON x=? :interrogation	x<CR><LF>	x:Synchronisation sate x=0 : synch. state OFF x=1 : synch. state ON
Set no Alarm Window	**AW**ddd<CR><LF>	ddd = Half no Alarm Window in µs. From 1 to 255 AW000 : no checking AW??? : interrogation	ddd<CR><LF>	ddd : half no Alarm Window in µs.
Set Tracking Window (in µs)	**TW**ddd<CR><LF>	ddd = half Tracking Window in µs. From 001 to 255 TW000 : no checking TW??? : interrogation	ddd<CR><LF>	ddd : half Tracking Window in µs.
Set tracking phase loop time constant	**TC**dddddd<CR><LF>	dddddd = Time constant in seconds (000100 to 999999) TC000000 : change to auto. TC?????? : interrogation	dddddd<CR><LF>	dddddd : time constant in seconds
Set frequency save. Average value, when Status = 2, 3	**FS**x<CR><LF>	x=0 : never save x=1 : save every 24 hours x=2 : save right now x=3 : save actual freq. now x=? : interrogation	x<CR><LF>	x=0 : never save x=1 : save every 24 hours
Set fine phase comparator Offset	**CO**sddd<CR><LF>	s :+/- signe ddd : limited with range + 127 / - 128 CO???? : interrogation	sddd<CR><LF>	s :+/- signe ddd : offset in approx 1 ns steps
Raw phase adjust	**RA**sddd<CR><LF>	s :+/- signe ddd : limited with range + 127 / - 128	sddd <CR><LF>	s :+/- signe ddd : raw phase just asked in 66 ns steps

Set PPSOUT Pulse Width (rounded to 66ns)	**PW**ddddddddd<CR><LF>	ddddddddd=pulse width in ns Max :999999933 PWOOOOOOOOO: no pulse PW?????????: interrogation	ddddddddd<CR><LF>	ddddddddd=pulse width in ns
Set PPSOUT delay (rounded to 66ns)	**DE**ddddddddd<CR><LF>	ddddddddd=delay in ns Max : 999999933 DEOOOOOOOOO : synch. to PPSREF DE????????? : interrogation	ddddddddd<CR><LF>	ddddddddd= delay in ns
Set Pulse Per d second	**PP**dddeee<CR><LF>	ddd: 1 pulse every ddd second eee: offset to GPS epoch in second PPOOOOOO : no pulse PP?????? : interrogation	dddeee<CR><LF>	ddd: 1 pulse every ddd second eee: offset to GPS epoch in second
Date	**DT** <CR><LF>		yyyy-mm-dd	yyyy : year mm : month dd : day
Set date	**DT** yyyy-mm-dd <CR><LF>	yyyy : year mm : month dd : day	yyyy-mm-dd	yyyy : year mm : month dd : day
Time of day	**TD**<CR><LF>	-	hh:mm:ss<CR><LF>	hh:hours mm:minutes ss:seconds
Set time of day	**TD**hh:mm:ss<CR><LF>	hh:Hours mm:Minutes ss:seconds	hh:mm:ss<CR><LF>	hh:hours mm:minutes ss:seconds
Set frequency correction	**FC**sddddd<CR><LF>	s=+/- signe ddddd = limited within range : +32767/-32768 FC?????? : interrogation	sddddd<CR><LF>	s: +/- signe ddddd : frequency in 5.12 x 10^{-13} step
Set module adjust	**MA**vxx..<CR><LF>	v : action verb xx: 00..FF: parameter number v=R : Read from ram v=W : Write to ram v=L : Load from eeprom v=S : Store to eeprom v=F : Flash value v=B : Behavior at start v=A : Activate msg at start v=C : Cancel msg at start v=H : Help v=T : Type of data	Various, see Manual	Various, see Manual

Pin-Out Status Levels

PIN # 4 & 5 STATUS LEVELS			
Status	Pin # 4 Xtal not locked to Rb line	Pin # 5 Track/Synch alarm	
	Rb lock (open collector)	In Track Mode (TTL + 1K)	In Synch Mode (TTL + 1K)
s=0 :warming up	Low (<.2 V / 5 mA)	High	High
s=1 :tracking set-up	High	High	High
s=2 :track to PPSREF	High	**Low**	High
s=3 :synch to PPSREF	High	High	**Low**
s=4 :Free Run. Track OFF	High	High	High
s=5 :FR. PPSREF unstable	High	High	High
s=6 :FR. No PPSREF	High	High	High
s=7 :FREEZE	High	High	High
s=8 :factory used	High	High	High
s=9 :fault or Rb OOL	Low (<.2 V / 5 mA)	High	High

NMEA 0183 Format (BTA, BTB, BTR, BTZ)

$PTNTA,yyyymmddhhnnss,q,**T3**,rrrrrrr,sfff,x,y*CS**<CR><LF>**
yyyy: year; mm:month; dd: day; hh: hour; nn: minute; ss: second; q: quality, 0: Rb line not locked, 1: Free Run, 2: Disciplined; T3: format descriptor; rrrrrrr: effective time interval PPSOUT vs PPSREF; sff: phase comparator; x,y: reserved; CS: checksum.

$PTNTS,B,s,ffff,iiii,aaaa,x,y,s,cccccc,ggg.gg,x,y*CS**<CR><LF>**
s: general GRClok-1500 status; ffff: actual frequency offset; iiii: integral part of PI regulator; aaaa: average frequency on 24 hours; x,y: reserved; cccccc: loop time constant; ggg.gg: sigma; x,y: reserved; CS: checksum.

$GPRMC,hhnnss.**OO**,v,tttt.tttt,h,nnnnn.nnnn,a,,,ddmmyy,,,**E***CS**<CR><LF>**
hhnnss: hour, minute, second(UTC); v: validity(**A/V**=valid); tttt.tttt: latitude(degree.minute); h: hemisphere(**N/S**); nnnnn.nnnn: longitude(degree.minute); a: area(**E/W**); ddmmyy: day, month, year; CS: checksum.

$GPZDA, hhnnss,dd,mm,yyyy,,*CS**<CR><LF>**
hhnnss: hour, minute, second(UTC); dd,mm,yyyy: day, month, year; CS: checksum.

PIN-OUT DESCRIPTION

Males D-Sub 25 Pins

Pin #	GRClok-1500	Dir
1	**12V**(11.2 to 16) or **24V** (20 to 32)	Input
2	**12V**(11.2 to 16) or **24V** (20 to 32)	Input
3	**GND**	Ret
4	**Rb lock** (open collector) (lock=open)	Output
5	**Track/Synch** Alarm (TTL+1K) (lock=0V)	Output
6	**FA** (analog frequency adjust input)	Input
7	**Vref out** (+5V internal reference)	Output
8	**NC** (PPSREF reference time pulse)	Input
9	**NC** (Factory use or diagnostics)	Output
10	**GND**	Ret
11	**OPTION** (PLL synthesizer output 0-5V CMOS > 20mA sink/source)	Output
12	**NC** (/RxD2 GPS, RS232 Receive 5V-0)	Input
13	**NC** (Option 2)	Output
14	**/Sync**(synchronize PPSOUT to PPSREF)	Input
15	**/Track** (PPSREF phase tracking)	Input
16	**NC** (/TxD2 GPS (RS232 Transmit 5V-0)	In-Out
17	**/Reset** (LNSRO micro controller)	Input
18	**TxD1** (RS232 Transmit 0-5V)	Output
19	**RxD1** (RS232 Receive 0-5V)	Input
20	**PPSOUT** (output time pulse from internal clock)	Output
21	**NC** (Time Tagging)	Ret
22	**GND**	Ret
23	**GND**	Ret
24	**NC** (RFOut in other iSync clock)	Output
25	**GND**	Ret

HEAT SINK MOUNTING

Below are some heat sink options depending on your environmental system configuration:

1) Mount the GRClok-1500 on a copper ground PCB. This mounting configuration is not recommended for >50°C ambient operational temperature.

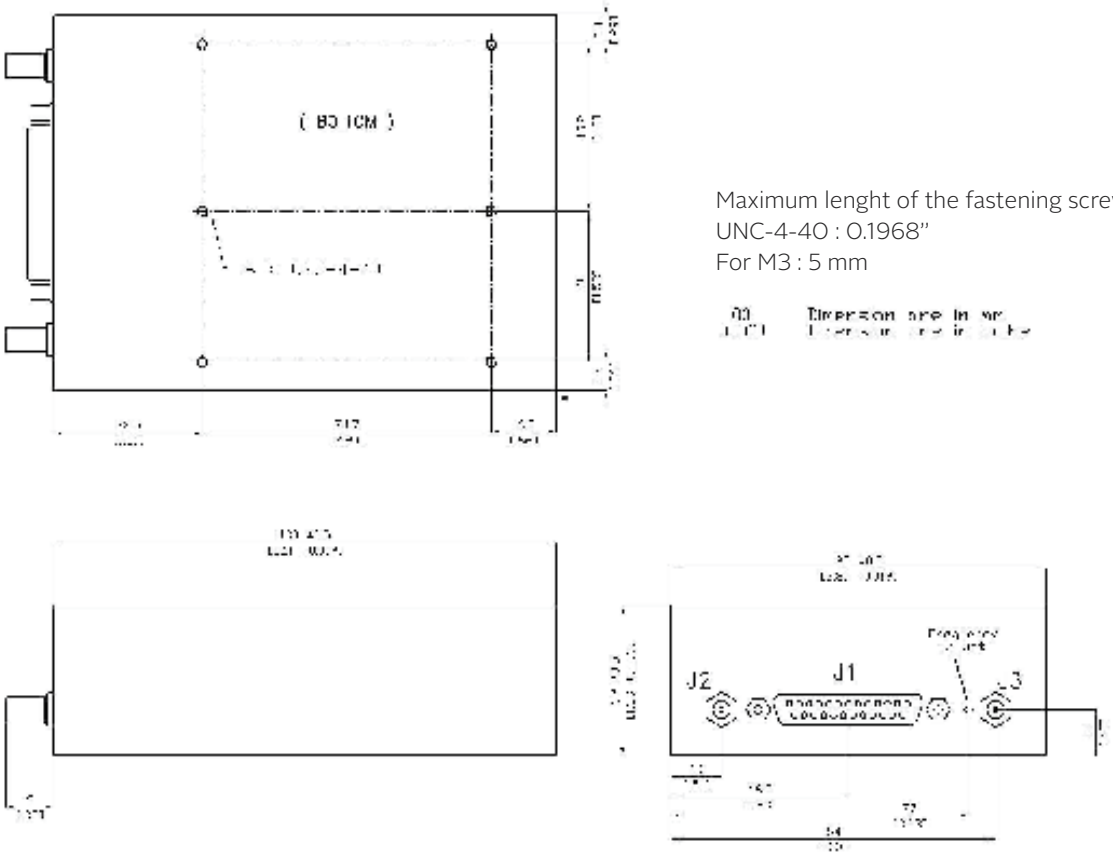
2) Mount the GRClok-1500 against a system chassis using the UNC 4-40, Option M3 (code 'M3') screws with the provided thermal pad or thermal paste in between and wire bridge the D-Sub connector. This mounting configuration is recommended.

3) Mount a radiator on top of the GRClok-1500 with the provided thermal pad or thermal paste in between, if no base plate or system chassis is available. This mounting configuration is recommended.

For any heat sink mounting questions, best practices or recommendations, please feel free to contact us at clocksupport@orolia.com

Mechanical Sizes

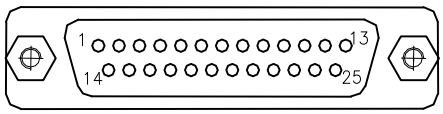
All sizes are in mm and the pictures are not to scale.



Maximum lenght of the fastening screws : For UNC-4-40 : 0.1968"
For M3 : 5 mm

Connector Front View

J1:



Male D-Sub 25 pins

J2: **SMA / RF out (10MHz)**

J3: **SMA / GPS Antenna**

30 August, 2022. Patented Smart GRClok-1500
Specifications subject to change or improvement without notice